IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	**MAIL STOP**
Jerome Assal et al.	Group Art Unit: 2815
Application No.: 10/524,891	Examiner: CHU,CHRIS C
Filed: October 31, 2005	Confirmation No.: 5889
For: FUNCTIONAL COATING OF AN SCFM PREFORM	

SECOND REQUEST FOR SUPPLEMENTAL NOTICE OF ALLOWABILITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants note with appreciation the receipt of a Post-Allowance Communication dated July 6, 2009. Attached to the communication, is an Examiner-initialed copy of a PTO 1449 Form originally filed February 16, 2005. However, certain references were lined through the Examiner-initialed copy, thereby indicating that these references have not been considered. Namely, foreign references JP 56-107352 and EP 0932201; and non-patent literature, the L. Krusin-Elbaum et al. article were lined through. In the correspondence of July 6, 2009 reference is made to "the attached signed copy." However, Applicants never received any such signed copy. Thus, no explanation is given as to why these references were not considered.

Subsequently, Applicants' representative contacted the Examiner via telephone on August 4, 2009. Applicants thank the Examiner for the courtesies extended to Applicants' representative during said telephone conference. In the telephone conference, the Examiner indicated that the record appeared to be

incomplete in that the image file wrapper also lacked any "signed copy." However, the Examiner orally indicated that the reason why these references were not considered is that copies had not been provided pursuant to 37 C.F.R. § 1.98.

In this regard, Applicants note that all three of the above-identified documents were listed on the International Search Report, and thus should have been transmitted to the USPTO as a designated office by the International Bureau. This belief is reflected in the enclosed copy of the first Information Disclosure Statement filed on February 16, 2005. Nevertheless, Applicants furnish herewith copies of the above-identified prior art documents for the Examiners convenience, along with a blank copy of the PTO 1449 Form originally filed on February 16, 2005. Applicants respectfully request that the Examiner initial the remaining foreign patent documents and non-patent literature documents identified above, and return the same to Applicants to complete the file.

If any questions, or possible deficiencies arise with respect to the above, it is respectfully requested that the undersigned be contacted so that any such issues may be adequately addressed and issuance of the above-identified patent application be expedited.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

Date: August 7, 2009

By: _____
Scott W. Cummings
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Attorney's Docket No. 004501-804

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Jerome Assal et al.	Group Art Unit:
Application No.: Unassigned	Examiner:
Filed: February 16, 2005	Confirmation No.:
For: FUNCTIONAL COATING OF THE SCFM PREFORM	

FIRST INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure as set forth in 37 C.F.R. § 1.56, the accompanying information is being submitted in accordance with 37 C.F.R. §§ 1.97 and 1.98.

The listed documents were cited in the International Search Report in the corresponding PCT application.

To assist the Examiner, the documents are listed on the attached form PTO-1449. However, copies of the documents are not provided as it is understood that they have already been transmitted by the International Bureau. It is respectfully requested that an Examiner initialed copy of this form be returned to the undersigned.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date February 16, 2005

By: M. Patrick Keane, Reg. No. 35,333
Patrick C. Keane
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10/524891

Substitute for form 1449A/PTO & 1449B/PTO

FIRST INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	DTO[redacted]c'd PCT/PTO 16 FEB 2005
Filing Date	February 16, 2005
First Named Inventor	Jerome Assal et al.
Examiner Name	
Attorney Docket Number	004501-804

U.S. PATENT DOCUMENTS

Examiner Initials	Document Number	Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Issue/Publication Date (MM-DD-YYYY)
	5,008,735		Edmond et al.	04-16-1991
	3,280,383		Emeis	10-18-1966
	4,816,424		Watanabe et al.	03-28-1989

FOREIGN PATENT DOCUMENTS

Examiner Initials	Document Number	Kind Code (if known)	Country	Date of Publication (MM-DD-YYYY)	STATUS						
					Translation	Partial Translation	Eng. Lang. Summary	Search Report	IPER	Abstract	Cited in Spec
	56-167352		Japan	12-23-1981				X		X	
	0 932 201		EP	07-28-1999				X			
								X			

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	L. KRUSIN-ELBAUM et al.; ZrN Diffusion Barrier in Aluminum Metallization Schemes; This Solid Film, 1983, pp. 81-87, Vol. 104; Elsevier Sequoia, Boston, Mass.

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with M.P.E.P. § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 56167352
PUBLICATION DATE : 23-12-81

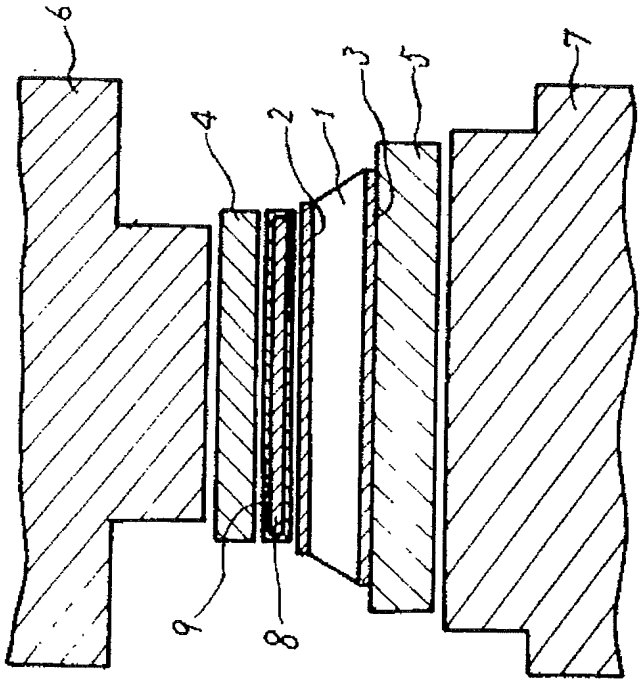
APPLICATION DATE : 26-05-80
APPLICATION NUMBER : 55070571

APPLICANT : MITSUBISHI ELECTRIC CORP;

INVENTOR : UEDA KAZUO;

INT.CL. : H01L 23/04 H01L 23/10

TITLE : PRESSURE-WELDING TYPE SEMICONDUCTOR DEVICE



ABSTRACT : PURPOSE: To prevent the breakage of a substrate and to reduce the variation of voltage drop value for the subject semiconductor device by a method wherein the metal plate having an Rh layer is placed between the Al main electrode located on the side of the main surface where no brazing exists and an Mo compensating plate in such manner that the Rh surface and the Al surface are facing each other.

CONSTITUTION: The main electrode 3 of the semiconductor substrate 1, whereon the Al main electrodes 2 and 3 are provided on both main surface, is brazed on the Mo compensating plate 5. On the side of the main electrode 2 of this device, the metal plate 8, whereon an Rh layer 9 was formed on the surface, (100~300μm or so in thickness) such as Ag, Cu and the like, for example, having an excellent malleability and a ductility and a high conductivity, is arranged in such manner that the Rh layer 9 is facing the Al surface. An Mo compensating plate 4 is placed so as to contact the metal plate 8 and the whole compensating plates 4 and 5 are contacted by pressuring the main electrode conductive materials 6 and 7 consisting of a copper pole. Through these procedures, the contacting characteristic of the device is improved and Al alloying reaction and the like is hardly generated, thereby enabling to prevent the breakage of the substrate as well as to reduce the variation of a voltage drop value.

Rh on Ag, Cu

⑲ 日本国特許庁（JP）　　⑪ 特許出願公開

⑫ 公開特許公報（A）　　昭56—167352

⑤1Int. Cl.³　識別記号　庁内整理番号
H 01 L 23/04　7738—5F
23/10

⑬公開　昭和56年(1981)12月23日

発明の数　1
審査請求　未請求

（全 4 頁）

⑤4加圧接触形半導体装置

⑦1出願人　機株式会社北伊丹製作所内
三菱電機株式会社
東京都千代田区丸の内２丁目２番３号

⑦4代理人　弁理士　葛野信一　外１名

⑵1特願　昭55—70571
⑵2出願　昭55(1980) 5 月26日

⑦2発明者　上田和男
伊丹市瑞原４丁目１番地三菱電

明　細　書

1. 発明の名称

加圧接触形半導体装置

2. 特許請求の範囲

(1) 第１の主面にアルミニウム膜からなる第１の主電極が形成され第２の主面にアルミニウム膜からなる第２の主電極が形成された半導体基体、延性および展性を有し導電性のよい金属材料からなり少なくとも一方の主面上にロジウム層が形成され上記ロジウム層が上記第１の主電極に接するようにして加圧接触させられる金属板、モリブデン板からなり上記金属板に加圧接触させられる第１の補償板、モリブデン板からなり上記第２の主電極にろう付けされた第２の補償板、上記第１の補償板に加圧接触させられて導電路を構成する第１の主電極導電体、および上記第２の補償板に加圧接触させられて導電路を構成する第２の主電極導電体を備えた加圧接触形半導体装置。

(2) 金属板にロジウム層の下地用ニッケル層が形成された金属板を用いたことを特徴とする特許請求の範囲第１項記載の加圧接触形半導体装置。

(3) 金属板にロジウム層の下地用銅層が形成された金属板を用いたことを特徴とする特許請求の範囲第１項記載の加圧接触形半導体装置。

(4) 金属板に銀板を用いたことを特徴とする特許請求の範囲第１項ないし第３項のいずれかに記載の加圧接触形半導体装置。

(5) 金属板に銅板を用いたことを特徴とする特許請求の範囲第１項ないし第３項のいずれかに記載の加圧接触形半導体装置。

(6) 金属板にアルミニウム板を用いたことを特徴とする特許請求の範囲第２項記載の加圧接触形半導体装置。

3. 発明の詳細な説明

この発明は加圧接触形半導体装置の改良に関するものである。

第１図は従来の加圧接触形半導体装置の一例の要部を示す断面図である。

図において、(1)は半導体基体であるシリコン(Si)ウエーハ、(2)はアルミニウム(Al)蒸着膜からなり

Si ウエーハ(1)の第1の主面上に形成された第1の主電極、(3)はAl蒸着膜からなりSi ウエーハ(1)の第2の主面上に形成された第2の主電極、(4)はモリブデン(Mo)板からなり第1の主電極(2)に加圧接触させられる第1の補償板、(5)はMo板からなり第2の主電極(3)にろう付けされた第2の補償板、(6)は銅柱からなり第1の補償板(4)に加圧接触させられて導電路を構成する第1の主電極導電体、(7)は銅柱からなり第2の補償板(5)に加圧接触させられて導電路を構成する第2の主電極導電体である。

ところで、このように構成された加圧接触形半導体装置では、Si ウエーハ(1)が動作時毎に発生する熱によつて、各構成部品が膨張と収縮とを繰返す。この膨張時、収縮時における応力によつて、Si ウエーハ(1)の第2の主電極(3)が第2の補償板(5)にろう付けされているので、Si ウエーハ(1)の第1の主電極(2)と第1の補償板(4)とが互いにこすり合うような運動をする。

第2図はSi ウエーハの第1の主電極と第1の補償板との接触状態を示す要部拡大断面図である。

第2図に示すように、Si ウエーハ(1)の第1の主電極(2)と第1の補償板(4)とが互いに接触するそれぞれの表面部に凹凸や反りがあるので、第1の主電極(2)と第1の補償板(4)とが均一に接触していない。このような接触状態で、第1の主電極(2)と第1の補償板(4)とが互いにこすり合う運動を続けているうちに、これらの接触面に、接触抵抗の小さい部分と大きい部分とが生ずるようになる。この接触抵抗の小さい部分に、Si ウエーハ(1)を流れる主電流がますます集中するようになり、極めて高い電流密度の領域が形成される。そうすると、例えば200～300kg/cm²程度の大きな圧接力の下では、この電流密度の高い領域に、第1の主電極(2)を構成するAlと第1の補償板(4)を構成するMoとが容易に融合してAl-Mo合金（図示イ）ができる。このようなAlとMoとの合金化が進むと、主電流通電時の電圧降下の値が初期値より変動したり、また、AlとMoとの合金化が進んだ部分に、上述の膨張時、収縮時における応力が集中して、Si ウエーハ(1)が破損したりすることがある。発明者の経験によれば、主電流を50時間通電すると、主電流通電時の電圧降下の値が初期値より10%以上変動し、かつSi ウエーハ(1)の破損が生じた。

この発明は、上述の問題点に鑑みてなされたもので、少なくとも一方の主面にAlと容易に合金化しないロジウム(Rh)層が形成され延性、展性を有し導電性のよい金属板を上記Rh層が半導体基体の第1の主面上に形成されAl膜からなる第1の主電極に接するようにして上記第1の主電極とMo板からなる第1の補償板との間に挿入することによつて、主電流通電時の電圧降下の値が初期値より変動することがなく、かつ半導体基体が破損しない加圧接触形半導体装置を提供することを目的とする。

第3図はこの発明の一実施例の要部を示す断面図である。

図において、第1図に示した従来例と同一符号は同様のものである。(8)は延性、展性を有し導電性のよい銀(Ag)、銅(Cu)、Alなどからなる金属板、(9)は金属板(8)の全表面上に電気メッキ法もしくは蒸着法で形成され、硬度が大きく、融点が高く、かつAlと容易に合金化しないRh層である。

この実施例の構成は、Rh層(9)が全表面上に形成された金属板(8)をSi ウエーハ(1)の第1の主電極(2)と第1の補償板(4)との間に挿入した以外は、第1図に示した従来例の構成と同様である。

この実施例では、表面上にRh層(9)が形成された金属板(8)を第1の主電極(2)に全加圧接触させ、この金属板(8)に第1の補償板(4)を加圧接触させたときに、第1の主電極(2)の表面部および第1の補償板(4)の表面部に凹凸や反りがあつても、これらの凹凸や反りに応じて金属板(8)が容易に塑性変形するので、Rh層(9)が第1の補償板(4)の表面および第1の主電極(2)の表面と均一に接触する。しかも、Rh層(9)と第1の主電極(2)を構成するAlとが容易に合金化しないので、第1図に示した従来例のように、主電流通電時の電圧降下の値が初期値より変動するようなことがなく、また、第1の補償板(4)、金属板(8)およびSi ウエーハ(1)の膨張時、

収縮時における応力によつて、Si ウエーハ(1)が破損するようなことがない。

発明者の実験によれば、外径が 85mm 程度の大きなSi ウエーハ(1)の第2の主電極(3)に第2の補償板(5)をろう付けした場合には、Si ウエーハ(1)の反りが 50 ～ 100μm 程度の大きなものになるので、Si ウエーハ(1)の第1の主電極(2)に金属板(8)を均一に加圧接触させ、この金属板(8)に第1の補償板(4)を均一に加圧接触させるためには、金属板(8)の厚さが少なくとも 100μm以上必要であつた。しかし、金属板(8)の厚さが 300μm以上になると、金属板(8)による主電流通電時の電圧降下の値が増大し、かつ金属板(8)の熱膨張係数とSi ウエーハ(1)の熱膨張係数との相違による影響が大きくなるので、金属板(8)の厚さとしては、100 ～ 300μm程度が適切であることがわかつた。また、金属板(8)がAg 板またはCu 板である場合には、これらのAg 板またはCu 板の表面上に直接電気メツキ法でRh 層(9)を形成すると、これらのAg 板またはCu 板とRh 層(9)との密着がよくなく、剝離が生じた。これを防止するために、Ag 板またはCu 板の表面上に、Cu のフラツシユメツキ法でCu の下地層を形成するか、またはニツケル(Ni)のメツキ法でNi の下地層を形成し、これらの下地層の表面上に電気メツキ法でRh 層(9)を形成し、更に温度 500℃ 程度の水素ガスの雰囲気中での30分間程度のシンター処理を施すことによつて、より一層大きい密着強度を得ることができた。なお、Cu またはNi の下地層の厚さは 0.1～0.5μm 程度でよく、これらの下地層の表面上に形成されるRh 層(9)の厚さは、0.05μm以下であると、Rh 層(9)を形成した効果がなく、0.8μm 以上であると、Rh 層(9)にクラツクやひび割れが生じやすくなるので、0.05 ～ 0.8μm 程度が適切であつた。

また、金属板(8)がAℓ 板である場合には、このAℓ 板の表面上に直接Ni メツキ法でNi の下地層を形成することができないので、このAℓ 板の表面部に市販のジンケート処理液で亜鉛置換層を形成し、この亜鉛置換層の表面上にNi メツキ法でNi の下地層を形成し、このNi の下地層の表面上に電気メツキ法でRh 層(9)を形成することができた。

このようにして形成されたRh 層(9)および金属板(8)を用いたこの実施例では、主電流を5000 時間通電しても、主電流通電時の電圧降下の値の変動や、Si ウエーハ(1)の第1の主電極(2)を構成するAℓ とRh 層(9)との剝着がみられず、Rh 層(9)の顕著な効果が確認された。

なお、この実施例では、金属板(8)の表面上の全面にRh 層(9)を形成したが、必ずしもRh 層(9)を金属板(8)の表面上の全面に形成する必要がなく、金属板(8)のSi ウエーハ(1)の第1の主電極(2)に加圧接触させられる側の表面にのみ形成するようにしても、この実施例と同様の効果がある。

以上、説明したように、この発明の加圧接触形半導体装置では、少なくとも一方の主面にAℓ と容易に合金化しないRh 層が形成され延性、展性を有し導電性のよい金属板を上記Rh 層が半導体基体の第1の主面上に形成されAℓ 膜からなる第1の主電極に接するようにして上記第1の主電極とMo 板からなる第1の補償板との間に挿入したので、上記第1の主電極の表面部および上記第1の補償板の表面部に凹凸や反りがあつても、これらの凹凸や反りに応じて上記金属板が容易に塑性変形するから、上記Rh 層が上記第1の補償板の表面および上記第1の主電極の表面と均一に接触する。しかも、上記Rh 層と上記第1の主電極を構成するAℓ とが容易に合金化しないので、従来例のように、主電流通電時の電圧降下の値が初期値より変動するようなことがなく、また、上記第1の補償板、上記金属板および上記半導体基体の膨張時、収縮時における応力によつて、上記半導体基体が破損するようなことがない。

4. 図面の簡単な説明

第1図は従来の加圧接触形半導体装置の一例の要部を示す断面図、第2図は上記従来例のSi ウエーハの第1の主電極と第1の補償板との接触状態を示す要部拡大断面図、第3図はこの発明の一実施例の要部を示す断面図である。

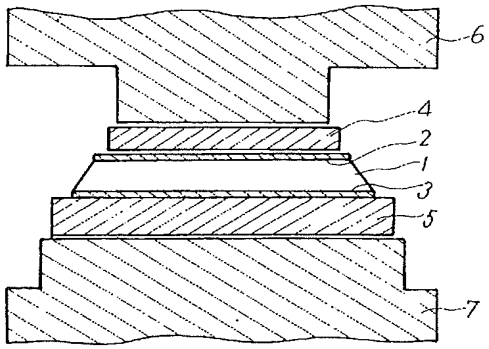
図において、(1)はSi ウエーハ（半導体基体）、

(2)は第1の主電極、(3)は第2の主電極、(4)は第1の補償板、(5)は第2の補償板、(6)は第1の主電極導電体、(7)は第2の主電極導電体、(8)は金属板、(9)はRh層である。

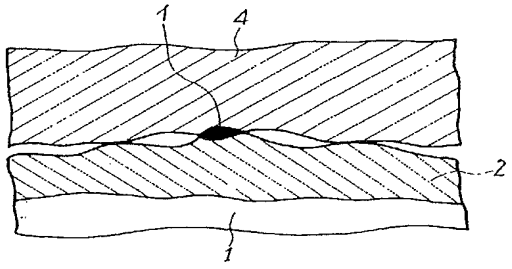
なお、図中同一符号はそれぞれ同一もしくは相当部分を示す。

代理人　葛野信一(外1名)

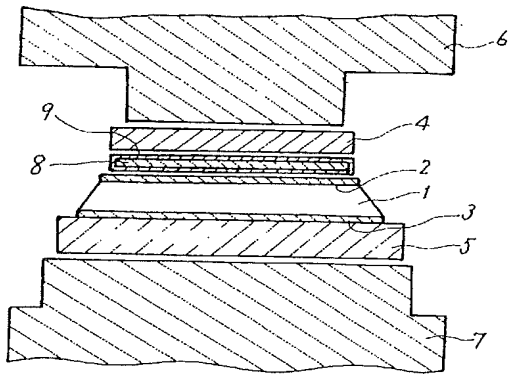
第1図



第2図



第3図



(19) Europäisches Patentamt
European Patent Office
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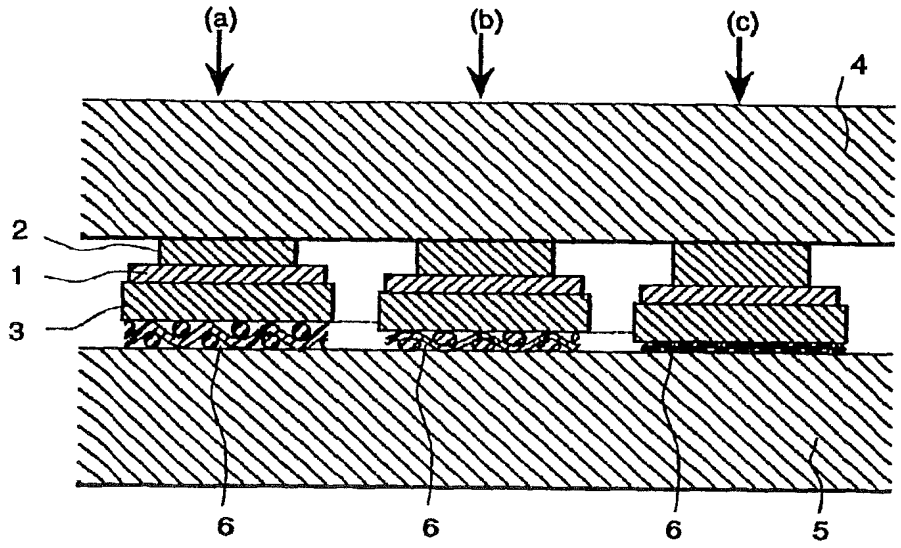
(54) Press contact type semiconductor device and converter using same

(57) In accordance with a press contact type semiconductor device, a metallic body 6 having macroscopic vacancies in its portion is arranged between a main electrode of the semiconductor device and a main electrode plate 5, or between an intermediate electrode plate 3 arranged on a main plain of the semiconductor element 1 and a main electrode plate 5, respectively.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a press contact type semiconductor device, particularly, to a press contact type semiconductor device capable of ensuring an uniform contact condition between semiconductor elements and package electrodes, and of decreasing thermal resistance and electrical resistance, and a converter using the same.

[0002] Technology of power electronics, wherein a main circuit current is controlled by using technology of semiconductor electronics, has been applied widely to various fields, and, furthermore, the applied fields have been still expanding. Semiconductor elements for power electronics are as follows: thyristor, light-triggered thyristor, gate-turn-off thyristor (GTO), insulated gate bipolar transistor (hereinafter, called IGBT) which is a MOS controlled device, metal oxide semiconductor field effect transistor (hereinafter, called MOSFET), and others. In these devices, main electrodes (cathode, emitter electrode) are formed on a first main plane of a semiconductor chip, and other main electrodes (anode, collector electrode) are formed on a second main plane of the semiconductor chip.

In the semiconductor devices for large power such as GTO, light-triggered thyristor, and the like, the semiconductor element is packaged per every wafer. The both main electrodes of the above element have a structure, wherein the main electrodes are contacted by pressing with a pair of external main electrode plates in the package via an intermediate electrode plate (buffer electrode plate for thermal stress) made of Mo or W. In order to improve uniformity of switching operation, large current turn-off capability, and the like, it is important to make contact conditions among the element electrodes, the intermediate electrode plates, and the external main electrode plates as uniform as possible, and to decrease contact thermal resistance and electrical resistance. Therefore, a countermeasure to decrease warps and waviness by improving precision (flatness, plainness) in manufacturing parts of the package has been generally adopted.

[0003] On the other hand, a plurality of chips have been mounted mainly by a package composition of wire-connecting electrodes type called a module type structure in IGBT and the like. In case of the module type package, heat generated in the internal of the element chip is released from only one side of the package (a plane which has not been connected by wire), that is, the side of the package where the electrode has been mounted directly on a base substrate. Accordingly, thermal resistance is generally significant, and the number of chips which can be mounted on a package, and an usable current capacity (an amount of heat generation, or a mounting density) were limited.

[0004] Currently, in order to solve the above problems and to respond to a demand for increasing the capacity, a semiconductor device having a press contacting structure of multichips in parallel, wherein a plurality of IGBT chips are assembled in parallel in a flat type package so as to be capable of taking out an emitter electrode and collector electrode formed on the main planes of each chips by plane-contacting to a pair of external main electrode plates provided at the package, such as disclosed in JP-A-8-88240 (1996) has been receiving attentions. In accordance with the semiconductor device having a press contacting structure of multichips in parallel, variations in height of each position of every chips caused by variation in dimensions of the members (parts), and variations in warps and waviness of the main electrode plate per location can not be avoided. Accordingly, the pressure varies per chip, and uniform contacts can not be obtained. Then, the thermal resistance and the electrical resistance per position of every chips varied remarkably, and a serious problem that the characteristics of the elements were unstable as a whole was remained. As the most simply, the problem can be solved by using the members having severely precise dimensions. However, the above countermeasure can not be deemed as realistic, because increasing a production cost and a selection cost of the members can not be avoided. For solving the above problem, JP-A-8-88240 (1996) discloses a method to insert a soft metallic sheet having a ductility such as silver as a thickness correcting plate.

[0005] The size of the element (wafer size) in the package of the GTO and the like will be increased for responding to the demand for increasing their capacities in the future. Accordingly, the warps, waviness, and the like of the package members (electrode members) are in a trend to be increased in accordance with increasing the diameter of the element. The countermeasure to decrease warps and waviness by improving precision in manufacturing parts of the package (flatness, plainness) as described previously has a limit in manufacturing, and a serious problem in cost. Accordingly, it becomes increasingly difficult to ensure an uniform contact between the wafer and the package members (electrodes) in the whole plane of the element size (wafer size), and to decrease the thermal resistance and the electrical resistance.

[0006] On the other hand, in accordance with the method of inserting a soft metallic sheet disclosed as a countermeasure for solving the problem of uniform contact between chips of the semiconductor device having a press contact structure of multichips in parallel as described previously, it has been revealed by study of the inventors of the present invention that the amount of deformation of the sheet is very little (deforming only by elastic deformation) with a pressure in the range of practical use, i.e. the pressure which does not destroy at least the semiconductor chip, and the amount of deformation is not sufficient for ensuring uniform contact when the variation in height per position of every chips

(and the height including the intermediate electrode members interposing the chip, and others) is remarkable.

[0007] The reason can be estimated that, when a pressure is added to a soft metallic sheet in a thickness direction to cause a plastic deformation in a lateral direction as indicated schematically in FIG. 25, deformation resistance in the lateral direction becomes extremely large, even if the soft metallic material is used, due to a friction force (friction resistance) 56 generated at the boundary between the electrode members 54, 55 interposing the soft metallic sheet 53. Even if the pressure is increased in order to cause a plastic deformation, the friction force is increased in proportion to the pressure, and the plastic deformation can not be readily caused. Particularly, in a case of a sheet form, wherein the area receiving the resistance is remarkably larger than the thickness, influence of the friction force generated on the surface of the area becomes dominant, and even if a pressure exceeding the yield stress of the material known to the public is added, substantial plastic deformation (flow) is not caused practically, and the thickness of the soft metallic sheet is scarcely changed before and after pressing.

[0008] The present invention is to provide a method for ensuring an uniform press contact condition on a large area region, which has been becoming more difficult than ever in accordance with increasing the size of the package by increasing the diameter of the wafer, and with connecting multichips in parallel of the element corresponding to increasing the capacity. That is, the present invention is to provide a method, which is capable of accommodating the variation in height of the contacting plane (warps, waviness, variation in dimensions of the members, and the like), and of decreasing the thermal resistance and electrical resistance at the contacting boundary planes. The second object of the present invention is to provided a converter preferable for a system of a large capacity by using the semiconductor device obtained by the above methods.

SUMMARY OF THE INVENTION

[0009] In accordance with the press contact type semiconductor device relating to the present invention, a semiconductor element comprising at least a first main electrode on a first main plane, and a second main electrode on a second main plane is assembled between a pair of main electrode plates, and a metallic body having macroscopic vacancies inside is arranged between electrodes of said semiconductor element and the main electrode plate.

[0010] Furthermore, in accordance with the press contact type semiconductor device having a practical composition relating to the present invention, a semiconductor element comprising at least a first main electrode on a first main plane, and a second main electrode on a second main plane is assembled between a pair of main electrode plates, and any one selected from at least a metallic netting, a plate manufactured to be uneven, and a porous metallic plate is arranged between electrodes of said semiconductor element and the main electrode plate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]

FIG. 1 is a schematic cross section indicating a fundamental composition of the present invention,
FIG. 2 is a set of schematic illustrations indicating models of deformation processes of metallic netting caused by pressing,
FIG. 3 is a graph indicating the effects of the pressure on the amount of deformation in the thickness direction or electrical resistance of the metallic netting,
FIG. 4 is a set of cross sections indicating examples of cross sectional structure of metallic plates manufactured to be uneven,
FIG. 5 is a set of photographs indicating appearances of the metallic plates manufactured to be uneven,
FIG. 6 is a set of schematic illustrations indicating models of deformation processes caused by pressing the metallic plates manufactured to be uneven,
FIG. 7 is a schematic cross section indicating an embodiment of the present invention applied to an IGBT,
FIG. 8 is a schematic cross section indicating an embodiment of the present invention applied to an IGBT,
FIG. 9 is a schematic cross section indicating an embodiment of the present invention applied to an IGBT,
FIG. 10 is a schematic cross section indicating an embodiment of the present invention applied to a wafer size semiconductor element,
FIG. 11 is a schematic cross section indicating an embodiment of the present invention applied to a wafer size semiconductor element,
FIG. 12 is a schematic cross section indicating an embodiment of the present invention,
FIG. 13 is a schematic cross section indicating another fundamental composition of the present invention,
FIG. 14 is a graph indicating the effects of the pressure on the amount of thickness change or electrical resistance of porous metallic plate,
FIG. 15 is a set of schematic enlarged illustrations indicating fine surface structures of the porous metallic materials,
FIG. 16 is a schematic cross section indicating a cross sectional structure of the porous metallic material, whereon a dense metallic layer is formed on the surface,

FIG. 17 is a schematic cross section indicating a cross sectional structure of the porous metallic material, whereon a dense metallic layer is formed on the surface,

FIG. 18 is a schematic cross section indicating an embodiment of the present invention applied to an IGBT,

FIG. 19 is a schematic cross section indicating an embodiment of the present invention applied to an IGBT,

FIG. 20 is a schematic cross section indicating an embodiment of the present invention applied to an IGBT,

FIG. 21 is a schematic cross section indicating an embodiment of the present invention applied to a wafer size semiconductor element,

FIG. 22 is a schematic cross section indicating an embodiment of the present invention,

FIG. 23 is a circuit diagram indicating composition of a bridge using the semiconductor device of the present invention,

FIG. 24 is a circuit diagram indicating a composition of self-commutated converter using four bridges of the three phase bridge indicated in FIG. 23, and

FIG. 25 is an illustration for explaining deformation behavior of the soft metal when it is pressed by a conventional method.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0012] A fundamental application state of the present invention is indicated in FIG. 1. At least a first main electrode is formed on a first main plane, and a second main electrode is formed on a second main plane in a semiconductor element 1. Intermediate electrode plates 2, 3 composed of Mo, W, and the like are arranged above the both main electrode planes, and furthermore, a pair of main electrode plates (common electrode plates) 4, 5 composed of Cu, or a Cu alloy are arranged at outer side portions of the intermediate electrode plates. In accordance with the present embodiment, a metallic body having macroscopic vacancies inside such as a metallic netting, or a metallic plate manufactured to be uneven 6, is inserted between the intermediate electrode plate 3 and the main electrode plate 5, and all the members are contacted each other by pressing the whole together. FIG. 1 indicates examples in the order of increasing the total height of the member 1, 2, and 3 by the position of (a), (b), and (c). Corresponding to these heights, the thickness of the metallic netting, or the metallic plate manufactured to be uneven 6, which were a definite thickness before the pressing, have been decreased in the order of (a), (b), and (c) by crushing and thinning. That means, the metallic netting, or the metallic plate manufactured to be uneven, is deformed by pressing so that the total heights including the height of the metallic netting, or the metallic plate manufactured to be uneven (a sum of the heights of the members 1, 2, 3, and 6) become equal at the positions of (a), (b), and (c), and their thickness is varied. Therefore, even in a case if each of the above members 1, 2, and 3 differs each other in thickness, and the main electrode plates 4, 5 have warps and waviness, the semiconductor element can be mounted with ensuring a desirable press contact state at the plural chip positions (a), (b), and (c), and a semiconductor device having less variation in thermal resistance and electrical resistance can be realized. In accordance with FIG. 1, an example wherein the metallic netting, or the metallic plated manufactured to be uneven 6 is inserted in the plane contacting with pressure facing to the main electrode plate 5 and the intermediate electrode plate 3 is indicated. However, the inserted position can be at other contacting planes such as between the main electrode plate 4 and the intermediate electrode plate 2, between the element 1 and the intermediate electrode plates 2, 3, and plural contacting planes can be used concurrently. Furthermore, the metallic netting different each other, or the metallic plates manufactured to be uneven different each other per each of the planes between the electrodes can be arranged.

[0013] FIG. 2 is a set of schematic illustrations indicating a model of deformation processes of the metallic netting 9 provided between the electrode plate 7 and the electrode plate 8 caused by pressing. FIG. 2 (a) indicates a contacting state before causing a large pressure deformation, (b) indicates a state during deformation under pressing, and (c) indicates a state after the deformation is completed thoroughly by the applies pressure. FIG. 3 indicates the effects of the pressure on the amount of deformation in the thickness direction of the metallic netting, that is a variation in thickness, or electrical resistance when the metallic netting is contacted between two electrodes with pressure.

[0014] In the states of FIG. 2 (a) and FIG. 3 (a), loading is too small, and the amount of deformation in the thickness direction of the metallic netting is small. Since the contacting electrical resistance between the electrode plate and the metallic netting depends significantly on the pressure, values of the electrical resistance is decreased remarkably in accordance with increasing the pressure. If further larger load is added, the metallic netting 9 provided between the electrode plate 7 and the electrode plate 8 is deformed significantly by compression as indicated in FIG. 2 (b) and FIG. 3 (b). That is, metallic wires (fiber) composing the metallic netting are deformed significantly with compression, and the thickness of the metallic netting is decreased. This is because the load is concentrated to the portion where the metallic netting is contacted with the electrode plates 7, 8, the pressure applied to this portion becomes extremely higher than the apparent pressure, and the metallic netting starts to be readily deformed by compression. Since the metallic netting has a large amount of openings, spatial restriction against the deformation of the pressed metal is

reduced, which is different from the case of a dense metallic foil (thin plate) indicated in FIG. 25, and the metallic netting is easily deformed by pressure. Accompanied with this deformation, the contacting area between the surface of the electrode plate 7 and the electrode plate 8 with the metallic netting is increased. Furthermore, since the amount of deformation of this portion is significant, oxide film on the surface of the metal is broken and a desirable contact with newly generated plane can be obtained. Therefore, the contacting boundary planes generated at this time are in a very closely contacting state. In accordance with this effect, the electrical resistance is decreased further.

[0015] After the deformation of the metallic netting is generated sufficiently, the pressure at the contacting plane is not increased so much even if the loading is increased, because the electrode plates 7, 8 and the metallic netting 9 are contacted with a large area. Furthermore, since the deformation resistance is increased by the same reason as indicated in FIG. 25, variation rate of the amount of deformation is decreased as indicated in FIG. 2 (c) and FIG. 3 (c). Theoretically, if an infinite loading can be added, the deformation until the interval between the boundary planes can be filled completely can be achieved. Practically, the interval can not be filled completely on account of the restriction of the loading and the like, and some portions are remained as uncontacted. However, the effect of the uncontacted portions to the electrical resistance is not significant, and a desirably small electrical resistance can be obtained. In accordance with observed results on the thermal resistance, approximately same behavior as the observed results on the electrical resistance was indicated.

[0016] The metallic netting referred to in the present invention includes, in addition to a sheet of netting woven with metallic fiber by various weaving manner, a sheet of netting woven with conductive fiber such as carbon fiber and the like, and a sheet material having a complex structure composed of an organic resin of core and a metal of surface layer. The material for the metallic fiber can be selected from the group consisting of soft metals having a small electrical resistance and thermal resistance such as copper, aluminum, silver, gold, and the like; significantly soft metal such as soldering material and the like; materials of inexpensive and superior in oxidation resistance such as nickel, stainless steel (SUS), and the like; and materials superior in high temperature characteristics as Ni base alloys and the like such as inconel and the like; and the material having the most suitable characteristics in consideration of the applied target can be selected. Corresponding to the amount of deformation, electrical resistance, and thermal resistance required in the region of necessary loading, optimization in using of various weaving manner such as plain weaving, twill weaving, plain tatami weaving, twill tatami weaving, and the like; various diameters of fiber; various mesh sizes; and others is desirable. Generally speaking, the amount of deformation can be increased if the diameter of the fiber is increased. On the other hand, in order to control the range of the loading wherein the deformation occurs, it is generally effective to decrease the mesh size for increasing the number of contacting points of the netting with the electrodes. Since the amount of deformation of the complex sheet material, wherein resin fiber is coated with metal, can be made larger than that of the sheet material made of metallic fiber, it is particularly effective in use, which requires a large amount of elastic deformation.

[0017] The metallic plate manufactured to be uneven referred to in the present invention means a metallic body, which is manufactured so as to have different thickness depending on positions, in contrast with conventional metallic plate, metallic foil, and metallic sheet, which generally mean a flat dense body having substantially an uniform thickness. Metallic plates called by various names such as expanded metal, meshed metal, grid metal, slit metal, punched metal, embossing manufactured plate, dimple manufactured plate, wave plate, and the like are included in the metallic plates of the present invention. Representative examples of shapes are indicated in FIG. 4 as the cross sectional shapes of the models, and examples of appearance photographs are indicated in FIG. 5 ((a) expanded metal, (b) slit manufactured plate, and (c) embossing manufactured plate).

[0018] As an example of metallic plate manufactured to be uneven, a model of deformation processes of a wave plate 10 caused by pressing is indicated in FIG. 6. FIG. 6 (a) indicates a contacting state before causing a significant deformation by pressure, (b) indicates a state during deformation, and (c) indicates a state after deformation has been occurred sufficiently by pressure. In accordance with increasing the load, the wave plate 10 provided between the electrode plate 7 and the electrode plate 8 is significantly deformed in a certain range of pressure, which is determined by the plate thickness, material of the plate, manufactured waving pitch, manufactured shape, and others. That means, the waving shape portion which has been manufactured to be uneven is deformed significantly by compressing, and thickness of the wave plate 10 is decreased. Different from the case of a dense metallic foil (thin plate) shown in FIG. 25, relatively large pressure deformation can re readily obtained, because a large number of spaces are existed around the portion manufactured to be uneven as much as manufactured to be uneven and the deformation of the pressed metal is scarcely restricted spatially. In accordance with the deformation, the contacting area of the surfaces of the electrode 7 and the electrode 8 with the wave plate 10 is increased. Furthermore, since the amount of deformation of this contact portion is significant, the oxide film on the surface of the metal is broken and a desirable contact with newly generated plane can be obtained. Therefore, the contacting boundary planes generated at this time are in a very

closely contacting state. In accordance with these effects, the electrical resistance and the thermal resistance is decreased significantly. After the wave plate 10 deformed significantly, the electrodes 7, 8 come to contact with the wave plate 10 by a remarkably large area, and the pressure per area is not increased so much even if the applied load is increased. Furthermore, the variation rate of the amount of deformation becomes small, because the deformation resistance is increased as same as the case shown in FIG. 25.

[0019] As the material for the metallic plate, the material having the most suitable characteristics corresponding to the applied target can be selected from the group consisting of copper, aluminum, silver, gold, soldering material, nickel, stainless steel (SUS), and various alloys such as Ni base alloys and the like as same as the previous case. Regarding the thickness of original plate manufactured to be uneven, and the depth and pitches of the manufacturing to make uneven, the most suitable conditions corresponding to the amount of deformation, electrical resistance, and thermal resistance required for the necessary pressure range can be selected. The most suitable material and surface processing are desirably selected depending on the using condition of the semiconductor device based on which must be prior to whether decreasing the thermal resistance and electrical resistance, or improving the deformation capability.

[0020] When ensuring the large amount of deformation is desirable, any of a method of arranging the metallic netting, or the metallic plates manufactured to be uneven into plural different positions between electrodes, and a method of arranging a combined assembly of plural metallic netting, or plural metallic plates manufactured to be uneven into an interval between electrodes is desirable. When the combined assembly of the plural metallic netting or the plural metallic plates manufactured to be uneven is used, a pre-treatment to assemble them into a body previously is effective.

[0021] Since these materials have elastic-plastic deformation capabilities, a return as much as the elastic deformation can be observed when the loading is discharged after deformed. However, the plastic deformation corresponding approximately to the variation in height among mounted members can be ensured. In case of re-pressing, sufficient contacts can be ensured with the same pressure as previous pressure utilizing the elastic deformation.

[0022] As a method for decreasing the contacting resistance between the metallic netting, or the metallic plate manufactured to be uneven with electrodes interposing them, forming a metallic layer, which is softer and more oxidation resistant than the metallic material of the metallic netting and the metallic plate, onto the surface of the metallic netting or the metallic plate by means such as printing, plating, and the like is desirable. Particularly, it is effective when a hard metallic material, or a readily oxidized metal is used. For instance, a Ni netting or a Ni plate manufactured to be uneven coated with a soft film made of Ag or Au, or a metallic netting or a metallic plate manufactured to be uneven made of Cu or Al having an oxidation preventing film made of Ag or Au at its surface is used.

[0023] Furthermore, as another method, a method of arranging a dense metallic foil onto the surface of the metallic netting, or the metallic plate manufactured to be uneven, and forming a body together can be used. For the above metallic foil, using a metallic foil which is softer and more oxidation resistant than the metallic material of the metallic netting and the metallic plate is effective. For instance, a metallic netting or a metallic plate manufactured to be uneven made of Cu or Al having a metallic foil made of any of Cu, Al, Ag, Au, and the like on its surface is used.

[0024] In order to realize correction of heights, and decrease of electrical resistance and thermal resistance most suitably, not only a metallic netting or a metallic plate manufactured to be uneven, but also a soft metallic foil can be arranged concurrently between the electrodes. For instance, a method for ensuring approximately same amount of deformation with the same loading even if the contacting areas differ each other by inserting an Au foil between the upper main electrode plate and the intermediate electrode plate, and inserting a metallic netting or a metallic plate manufactured to be uneven between the lower main electrode plate and the intermediate electrode plate is effective.

[0025] FIG. 7 indicates an embodiment of the present invention applied to a reverse conductive type switching device, wherein a flywheel diode(FWD) 12 connected to a switching device using IGBT 11 in reverse parallel is integrated. FIG. 7 indicates a partial cross section from outer most portion of the press contact type semiconductor device at right side to the middle portion toward the center. In accordance with the IGBT chip 11, an emitter electrode is formed on almost whole plane of a first main plane at upper side, a collector electrode is formed on a second main plane at lower side, and, furthermore, an electrode for controlling (gate electrode) is formed on the first main plane. In accordance with the FWD 12, an anode electrode is formed on the upper plane of the silicon substrate, and a cathode electrode is formed on the lower plane of the silicon substrate. Each of these semiconductor chips is arranged on an integrated intermediate electrode 14 made of Mo, which operates to remove heat and concurrently to connect electrically, and, furthermore, is arranged so as to contact with each of the main electrodes on the chips via each intermediate electrode 13 per respective of the chips. This composition is further interposed between a first common main electrode plate (Cu) 4 and a second common main electrode plate (Cu) 5. A wave plate 17 made of Cu, i.e. a metallic plate manufactured to be uneven, is inserted between the intermediate electrode 13 and the common main electrode plate 4. An Au

plated film 15 is formed on the surface of the intermediate electrode plate by approximately 1 μm in thickness, and a Ni plated film 16 is formed on the surface of the common electrode plate by approximately 1-3 μm in thickness. The above semiconductor chips and the intermediate electrode are fixed mutually by a frame 24. A lead wire is taken out from the gate electrode 18 of the IGBT chip 11 by a wire bond 19, and is connected to the gate electrode wiring plate 20 formed on the intermediate electrode 14. An interval between the above pair of common main electrode plate 4, 5 is insulated externally by an insulating outer cylinder 21 made of ceramics and the like, and a hermetic structure is formed at an interval between the common main electrode plate and the insulating outer cylinder by sealing inside the package by a metallic plate 22. The gate electrode lead is taken out to outside the package by a sealed wiring 23 through the external cylinder 21.

[0026] The above wave plate 17 used in the present embodiment was made of Cu, its wave pitch was 1 mm, the thickness of the plate was 0.3 mm, and its surface was thin gold plated. The whole thickness of the wave plate including the initial uneven portion was 0.6 mm. Variation in thickness of the intermediate electrode plate mounted practically in the present embodiment was 100 μm at maximum. However, results of determining pressure distribution by inserting pressure sensitive paper between the intermediate electrode plate 14 and the chips 11, 12 revealed that the pressure difference was small, and they were pressed almost uniformly.

[0027] FIG. 8 indicates an embodiment of the present invention applied to a reverse conductive type switching device, wherein a MOS control type switching device 11 and a flywheel diode 12 are integrated. Main electrodes (collector, cathode) at lower side of each of these semiconductor chips are made of Au, and are connected to an intermediate electrode 14, whereon an Ag plated film 15 of 2-3 μm thick is formed previously, by heating and pressure welding. On the other hand, main electrodes (emitter, anode) at upper side of each of these semiconductor chips are made of Al, and are connected to an intermediate electrode 13, whereon an Au plated film 15 of 1-2 μm thick is formed previously. In accordance with the present embodiment, the above integrated intermediate bodies of electrodes and semiconductor chips are arranged in parallel between a first common main electrode plate (Cu) 4, a Ni plated film 16 of 2-4 μm thick is formed on its surface previously, and a second common main electrode plate (Cu) 5. In this case, an expanded metal plate 17 was inserted as the metallic plate manufactured to be uneven between the intermediate electrode 14 and the common main electrode plate 5, and the whole body was pressed via both of the common main electrode plates 4, 5.

[0028] The expanded metal plate 17 was made of Ag, thickness of the metal plate was approximately 0.1 mm, approximately 3000 mesh, and the whole thickness including the initial uneven portion was approximately 0.25 mm. Variation in thickness at each position of the chips mounted practically in the present embodiment was 80 μm at maximum. However, results of determining pressure distribution by inserting pressure sensitive paper between the intermediate electrode plate 13 and the common main electrode plate 4 revealed that the pressure difference was small, and they were pressed almost uniformly.

[0029] FIG. 9 indicates an example of mounting state, wherein a pin 25 for taking out a gate control electrode from the chip is formed at the center of the chip. FIG. 9 indicated an embodiment of the present invention applied to a reverse conductive type switching device, wherein a flywheel diode (FWD) 12 connected to a switching device using IGBT 11 in reverse parallel was integrated, as same as shown in FIG. 7. Main electrodes (collector, cathode) at lower side of each of these semiconductor chips are made of Au, and are connected to an intermediate electrode 14, whereon an Ag plated film of 2-3 μm thick is formed previously, by heating and pressure welding. On the other hand, the surface of the intermediate electrode 13 is plated with an Au film 15 of 2-3 μm thick, and is connected to each of the semiconductor chips by press contact. The above integrated bodies of electrodes and semiconductor chips are inserted between a first common main electrode plate (Cu) 4 and a second common main electrode plate (Cu) 5. In this case, in order to absorb the variation in height, complex metallic netting 17 composed of double-overlapped netting manufactured in a shape having a hole at the center are arranged around the pin 25 and a member 26 for insulating the pin between the intermediate electrode plate 13 and the common electrode plate 4. In accordance with this method, shifting the location of respective complex netting 17 can be prevented by the member 26 for insulating the central pin, and an assembling operation can be performed easily.

[0030] The complex netting composed of double-overlapped metallic netting can be integrated to a body at their peripheral portion by stamping the double-overlapped netting to a designated shape using a die, and the complex netting can be handled as a single complex netting component.

[0031] The gate circuit 27 is contained in a groove 28 provided to the first common main electrode plate (Cu), taken out to the periphery of the package, and further taken out by the wire 29, 23 to outside the package. In accordance with the present embodiment, the complex netting made of Cu was used, and its surface was plated with Au in order to decrease the contacting resistance, further. Accordingly, the contacting resistance between the intermediate electrode plate and the common electrode plate could be decreased significantly. The above effect was remarkable in the region where the pressure was small. Variation in thickness at each position of the chips mounted practically in the present embodiment was 200 μm at maximum. How-

ever, results of determining pressure distribution by inserting pressure sensitive paper between the intermediate electrode plate 14 and the common main electrode plate 5 revealed that the pressure difference was small, and they were pressed almost uniformly.

[0032] As explained above, in the case when various kinds of semiconductor chips are arranged in parallel and mounted in a package, and their thickness are varied significantly depending on their kind, a following method is effective; that is, the intermediate electrode plates having various average thickness depending on the kinds of the chips are prepared; remarkable difference of the thickness of the chips are adjusted with the intermediate electrode plates; furthermore, the metallic netting, or the metallic plate manufactured to be uneven of the present invention is used for accommodating the variation in height of the intermediate electrode plates and the semiconductor chips.

[0033] FIG. 10 indicates an embodiment of the present invention applied to a GTO. A semiconductor element substrate 31 is made of silicon (Si), and has at least a PN junction inside. Cathode electrodes and gate electrodes made of aluminum (Al) are formed on one of main planes of the semiconductor element substrate 31, and anode electrodes made of aluminum (Al) are formed on another main plane. Intermediate electrode plates 32, 33 made of molybdenum (Mo) are arranged on the upper side of the cathode electrode and the anode electrode, respectively. Metallic netting 34, 35 made of Cu were arranged between the intermediate electrode plates 32, 33 and a pair of external main electrode plates 4, 5 made of copper (Cu), and the whole body was pressed. A cap member 36 is arranged at side planes of the semiconductor element substrate 31. A part of gate lead 37 is arranged and contacted on the gate electrode on the semiconductor substrate, and the part is contacted with the gate electrode by pressing with the gate insulator 38 and a disc spring 39. All the above parts are arranged in a sealed package surrounded by an insulator 40, a pair of external electrodes 4, 5, and a flange 41. Another end of the gate lead 37 is taken out outside the insulator 40 via a sealing structure as a gate terminal.

[0034] FIG. 11 indicates an embodiment, wherein a punching metal 42 made of Cu, a dense Ag thin film layer is formed on its surface, is arranged between a cathode electrode side of a semiconductor element 31 of wafer size and an intermediate electrode plate 32. A metal foil 43 of Mo and an intermediate electrode plate 33, each of which is plated with Ag respectively, were arranged between an anode electrode side of the semiconductor element 31 and a common electrode plate 5. The variation in height could be absorbed with the punching copper plate 42 better than a flat copper plate, and contacting resistance could be decreased.

[0035] FIG. 12 indicates an embodiment, wherein no intermediate electrode plate is inserted between a collector side electrode of the semiconductor chip 1 and a main electrode plate 5. In order to prevent rupture by pressing the semiconductor element, a metallic netting, or a metallic plate manufactured to be uneven was arranged between an intermediate electrode plate 2 and a main electrode plate 4 of emitter side. In accordance with the present embodiment, an embossed plate 44 manufactured to have slits was used as the metallic plate manufactured to be uneven. A soft metal foil 45 was inserted between a chip main electrode and a main electrode plate 5, in order to decrease further contacting resistance and to protect the chips.

[0036] Conventionally, surface of the common electrode plate, and the intermediate electrode plate have been necessarily finished to make their maximum surface roughness (Rmax) less than 1 μm, in order to decrease their contacting resistance. However, even if surface of the common electrode plates and the intermediate electrode plates, which interposes the metallic netting, or metallic plate manufactured to be uneven, soft metal foil, and the like, is coarse such that its maximum surface roughness (Rmax) exceeds 1 μm, the material is deformed matching with uneven shape of the surface, and contacting area is increased microscopically and contacting resistance can be decreased. Therefore, production cost can be decreased.

[0037] As the material for the intermediate electrode, a material having a thermal expansion coefficient at a middle of Si and a material of the external main electrode, and a desirable thermal conductivity and electrical conductivity is used. Practically, a single metal such as tungsten (W), molybdenum (Mo), or complex material or alloys containing these element as a main composition material such as Cu-W, Ag-W, Cu-Mo, Ag-Mo, Cu-FeNi, and the like, a complex material of metal with ceramics or carbon, for instance, such as Cu/SiC, Cu/C, Al/SiC, Al/AlN, Cu/Cu_2O, and the like are desirable.

[0038] On the other hand, as the material for the main electrode, a conductive material having a desirable thermal conductivity such as copper, aluminum, and their alloys, for instance, using Cu-Ag, Cu-Sn, Cu-Zr, Cu-Zr-Cr, Cu-Ni-Si-Zr, and the like, or the above complex materials are desirable.

[0039] FIG. 13 indicates another applying state of the present invention. At least a first main electrode is formed on a first main plane of a semiconductor element 1, and a second main electrode is formed on a second main plane. Intermediate electrode plates 2, 3 made of Mo, or W and others are arranged on both of the main electrode planes, and furthermore, common electrode plates (main electrode plate) 4, 5 made of a pair of copper, and the like, are arranged at outer portions of the intermediate electrode plates. A porous metallic plate 6, as an example of metallic body having macroscopic vacancies inside, is inserted between the intermediate electrode plate 3 and the main electrode late 5, and each of the members are contacted by pressing its whole body together. FIG. 13 indicates a case when a sum of the heights of the members 1, 2,

and 3 is increased in the order at the positions of (a), (b), and (c). Corresponding to the difference of these heights, the thickness of the porous metallic plates 6 are decreased in the order of (a), (b), and (c) after contacting with pressure, although their thickness before contacting have been same. That means, the thickness of the porous metallic plate has been varied so as to make the whole height including the height of the porous metallic plate (a sum of the members 1, 2, 3, and 6) equal at the positions of (a), (b), and (c). Therefore, even if each of the members 1, 2, and 3 has various thickness, and even if the main electrode plates 4, 5 have warps and waviness, a preferable contacting state with pressure can be ensured at plural chip positions (a), (b), and (c), and the semiconductor chips can be mounted with the preferable contacting state. Accordingly, a semiconductor device having less variation in thermal resistance and electrical resistance can be realized . In accordance with FIG. 13, an embodiment, wherein the porous metallic plate 6 is inserted between contacting planes with pressure facing to the main electrode plate 5 and the intermediate electrode plate 3, is indicated. However, the inserting position can be varied to other contacting planes, such as between the main electrode plate 4 and the intermediate electrode plate 2, between the element 1 and the intermediate electrode plates 2, 3, and plural boundary planes can be used concurrently. Furthermore, various porous metallic plates made of different material each other can be arranged at respective of intervals between the electrodes.

[0040] The porous metal referred to in the present invention is metallic material including a large number of voids, while terminology of metallic plate, metallic foil, and metallic sheet mean in general substantially dense metallic members. The porous metal has a fine structure, wherein three dimensional random network of continuous metallic portions is formed. Examples of the porous metal include foamed metal, sponge metal, porous metal, foam metal, and the like. In accordance with the target of the present invention, the soft materials having a small electrical resistance and thermal resistance such as copper, aluminum, silver, gold, and the like, and materials of inexpensive and superior in oxidation resistance such as nickel, stainless steel (SUS), and the like are preferable in particular, and the material having the most suitable characteristics in consideration of the applied target can be selected.

[0041] FIG. 14 indicates the effects of the pressure on the amount of deformation (the amount of change in the thickness of porous metallic plate) and electrical resistance, determined by using a porous Cu plate (foamed metal copper plate) as the representative of the porous metallic plate. As a comparative example, a case when a conventional dense thin Cu plate is used is concurrently indicated in FIG. 14. The foamed metal copper plate is prepared by the steps of; forming a coated film of copper powder on surface of vacancies in foamed urethane by dry adhesion method; removing the urethane by thermal processing; and sintering the copper powder in a reducing atmosphere. The foamed metal copper plate is a porous copper metal plate having a three dimensional network skeleton of copper. Another method , wherein Cu coating film is formed on surface of foamed resin by a wet plating method, is similarly usable. Thickness of the porous Cu plate is decreased accompanied with increasing pressure. The porous Cu plate is deformed significantly in a specific pressure region (approximately 0.5 - 2 kg/mm^2), and the amount of deformation is decreased accompanied with increasing its density. The electrical resistance is decreased with increasing the pressure, and is changed significantly in the specific region of remarkable deformation of the porous Cu plate. On the contrary, in case of Cu thin plate, significant deformation caused by plastic deformation is not generated even if a pressure exceeding its yield stress is applies as explained previously (FIG. 25), but only minor deformation as much as elastic deformation is generated. Electrical resistance is decreased gradually, because contact resistance with measuring electrode is decreased in accordance with increasing pressure.

[0042] In case of the porous metal, different from the case of dense metal foil (thin plate) (FIG. 25), a large deformation can be occurred by relatively small pressure, because the porous metal itself has vacancies at its interior portion, and microscopically the material pressed with a force can be moved easily to these vacancies. The deformation is occurred substantially only in a thickness direction (a pressing direction), because the porous metal itself has vacancies, which make it possible to absorb the deformation, at its interior portion, and deformation resistance by friction in a lateral direction at the contacting planes. Accordingly, the porous metal after the deformation has less vacancies than the initial period, and becomes dense. The shape of the vacancy is varied to be flatten in the thickness direction. As described above, the material of the present invention makes it possible to decrease electrical resistance and thermal resistance effectively with ensuring an capability to cause significant deformation to the thickness direction, because the material of the present invention has a feature that metallic channel portion particularly in the thickness direction is more increased by deformation with pressure in comparison with the lateral direction. When conventional dense material is deformed (decreasing its thickness) significantly, the material as much as its changed volume flows plastically in the lateral direction, and a phenomenon that side plane of the material is swelled remarkably can be observed. However, when the porous material is used, its side plane is scarcely swelled even if it is deformed (decreasing its thickness) significantly, because the porous metal itself has sufficient vacancies, which makes it possible to absorb the deformation of the material, at its interior portion. Therefore, since

any problems such as contacting with adjacent material are not generated, the porous material is suitable for high density mounting.

[0043] Since these materials have elastic-plastic deformation capabilities, a return as much as the elastic deformation can be observed when the loading is discharged after deformed. However, the plastic deformation corresponding approximately to the variation in height among mounted members can be ensured. In case of re-pressing, sufficient contacts can be ensured with the same pressure as previous pressure utilizing the elastic deformation. Furthermore, since the porous material has a lower apparent elastic coefficient than the conventional dense material on account of the presence of voids, the amount of elastic deformation is large, and the porous material is suitable for maintaining a certain contacting state. The pressure causing the deformation, and the elastic-plastic deforming behavior can be controlled by the thickness, density (fraction of the vacancies), and material of the continuous portion of metal formed in three dimensions. These factors can be selected so as to cause the deformation by an appropriate pressure in accordance with the using condition.

[0044] When ensuring a large amount of deformation is desired, a large fraction of vacancy in the porous metallic material before the deformation is desirable, larger than 50 % is desirable, and particularly a range of 60-80 % is preferable. However, when the amount of deformation is not desired to be excessively large in view of operability based on its use, it is desirable to adjust the porous plate to have an optimum amount of deformation, thermal resistance, and electrical resistance in view of its use by decreasing the void fraction (densification) by pressing previously with a designated pressure.

[0045] As indicated in FIG. 14, the contacting resistance (electricity, heat) in the practical using condition at a boundary with the electrodes interposing the porous metallic plate becomes an important factor. In order to decrease the contacting resistance further, it is important to make the contacting resistance at the boundary with the electrodes interposing the porous metallic plate small as possible. Therefore, a microscopic shape at the outermost surface of the porous metallic plate is more desirable to be a structure shown in FIG. 15 (b), which has a large number of terminal parts in approximately parallel to the contacting surface, or of terminal parts 8 having a large declining angle as possible, than a structure shown in FIG. 15 (a), which has a large number of columnar metal 7 extruding perpendicularly to the contacting surface.

[0046] As another state of the porous metallic plate for decreasing the contacting resistance of the porous metallic plate with electrode materials interposing the porous metallic plate, it is effective to make the surface of the porous metallic plate denser than its internal portion to increase microscopic contacting area with the electrode material. Embodiments are indicated in FIG. 16 and FIG. 17. FIG. 18 indicates an embodiment, wherein a metallic layer 9, which is softer and more oxidation resistant than the metallic material of the porous metallic plate, is formed onto the surface of the porous metallic plate 6 by means such as printing, plating, and the like. For instance, a porous metallic plate made of Ni coated with a soft film made of Ag or Au, or a porous metallic plate made of Cu or Al having an oxidation preventing film made of Ag or Au at its surface is used. FIG. 17 (a) indicates an embodiment, wherein a dense metallic foil 10 is arranged onto the surface of porous metallic plate 6 and a body is formed together. For the above metallic foil, using a metallic foil which is softer and more oxidation resistant than the metallic material of the porous metallic plate, in addition to the same material as the porous metallic material, is effective. For instance, a porous metallic plate made of Cu or Al having a metallic foil made of any of Cu, Al, Ag, Au, and the like on its surface is used. FIG. 17 (b) indicates a cross section of a plate obtained by punching out from the material indicated in FIG. 17 (a) with a pressing machine. Because the end planes are crushed when pressing is performed, the porous metallic plate becomes a shape that side planes are also covered with the surface foil. Therefore, the above method is simple and convenient method for a case when side planes of the porous metallic plate are desirably protected with a dense film. As further another method, a method for increasing its density only at the surface of the porous metallic plate by exposing it to a high temperature for a short time can be used.

[0047] FIG. 18 indicates an embodiment of the present invention applied to a reverse conductive type switching device, wherein a flywheel diode (FWD) 12 connected to a switching device using IGBT 11 in reverse parallel is integrated. FIG. 18 indicates a partial cross section from outermost portion of the press contact type semiconductor device at right side to the middle portion toward the center. In accordance with the IGBT chip 11, an emitter electrode is formed on almost whole plane of a first main plane at upper side, a collector electrode is formed on a second main plane at lower side, and, furthermore, an electrode for controlling (gate electrode) is formed on the first main plane. In accordance with the FWD 12, an anode electrode is formed on the upper plane of the silicon substrate, and a cathode electrode is formed on the lower plane of the silicon substrate. Each of these semiconductor chips is arranged on an integrated intermediate electrode 14 made of Mo, which operates to remove heat and concurrently to connect electrically, and, furthermore, is arranged so as to contact with each of the main electrodes on the chips via each intermediate electrode 13 per respective of the chips. This composition is further interposed between a first common main electrode plate (Cu) 4 and a second common main electrode plate (Cu) 5. A porous copper plate 17 is inserted between the intermediate electrode 13 and the common main

electrode plate 4. An Au plated film 15 is formed on the surface of the intermediate electrode by approximately 3-5 μm in thickness, and a Ni plated film 16 is formed on the surface of the common electrode plate by approximately 1-3 μm in thickness. The above semiconductor chips and the intermediate electrode are fixed mutually by a frame 24 made of teflon . A lead wire is taken out from the gate electrode 18 of the IGBT chip 11 by a wire bond 19, and is connected to the gate electrode wiring plate 20 formed on the intermediate electrode 14 . An interval between the above pair of common main electrode plates 4, 5 is insulated externally by an insulating outer cylinder 21 made of ceramics and the like, and a hermetic structure is formed at an interval between the common main electrode plate and the insulating outer cylinder by sealing inside the package by a metallic plate 22. The gate electrode lead is taken out to outside the package by a sealed wiring 23 through the external cylinder 21.

[0048] The above porous copper plate was prepared by the steps of; forming a sheet from Cu powder slurry by doctor blade method, calcining the sheet for removing organic binder components, and reducing and presintering the Cu powder so as to remain voids at a higher temperature. Initial void fraction was 60 %, average void diameter was 30 μm, and thickness was 150 μm. Variation in thickness of the intermediate electrode plate mounted practically in the present embodiment was 50 μm at maximum. However, results of determining pressure distribution by inserting pressure sensitive paper between the intermediate electrode plate 14 and the chips 11, 12 revealed that the pressure difference was small, and they were pressed almost uniformly.

[0049] FIG. 19 indicates an embodiment of the present invention applied to a reverse conductive type switching device, wherein a MOS control type switching device 11 and a flywheel diode 12 are integrated. Main electrodes (collector, cathode) at lower side of each of these semiconductor chips are made of Au, and are connected to an intermediate electrode 14, whereon an Ag plated film 15 of 2-3 μm thick is formed previously, by heating and pressure welding. On the other hand, main electrodes (emitter, anode) at upper side of each of these semiconductor chips are made of Al, and are connected to an intermediate electrode 13, whereon an Au plated film 15 of 1-2 μm thick is formed previously. In accordance with the present embodiment, the above integrated intermediate bodies of electrodes and semiconductor chips are arranged in parallel between a first common main electrode plate (Cu) 4, an Ag plated film 16 of 2-4 μm thick is formed on its surface previously, and a second common main electrode plate (Cu) 5. In this case, a porous Ni plate 17 was inserted between the intermediate electrode 14 and the common main electrode late 5, and the whole body was pressed via both of the common main electrode plates 4, 5.

[0050] The porous Ni plate 17 was obtained by the steps of; processing foamed resin for making it have conductivity, plating with electrolytic Ni, heat treating for removing the foamed resin by burning. This material was further pressed to be formed as a plate material having a void diameter of approximately 0.2 mm, the number of cells of 60 pieces/inch, thickness of the metallic channel portion of 40-80 μm, plate thickness of 0.6 mm, and void fraction of approximately 80 %. In accordance with the present embodiment, the contacting resistance between the porous Ni plate and the above electrodes is reduced significantly, because both of the surfaces of electrodes at both sides interposing the porous Ni plate are plated with Ag. Variation in thickness at each position of the chips mounted practically in the present embodiment was 100 μm at maximum. However, results of determining pressure distribution by inserting pressure sensitive paper between the intermediate electrode plate 13 and the common main electrode plate 4 revealed that the pressure difference was small, and they were pressed almost uniformly.

[0051] In order to realize correction of the height and decrease of the electrical resistance and the thermal resistance at optimum, not only the porous metallic plate, but also soft metal foil can be inserted concurrently between the electrodes. For instance, a following method is effective; wherein an Au foil is inserted between the upper main electrode plate and the intermediate electrode plate, and a porous Ni plate is inserted between the lower main electrode plate and the intermediate electrode plate, for ensuring approximately same amount of deformation with a same loading even in a case when the contacting areas differ each other.

[0052] FIG. 20 indicates an example of mounting state, wherein a pin 25 for taking out a gate control electrode from the chip is formed at the center of the chip. FIG. 20 indicated an embodiment of the present invention applied to a reverse conductive type switching device, wherein a flywheel diode (FWD) 12 connected to a switching device using IGBT 11 in reverse parallel was integrated, as same as shown in FIG. 18. Main electrodes (collector, cathode) at lower side of each of these semiconductor chips are made of Au, and are connected to an intermediate electrode 14, whereon an Ag plated film of 2-3 μm thick is formed previously, by heating and pressure welding. On the other hand, the surface of the intermediate electrode 13 is plated with an Au film 15 of 2-3 μm thick, and is connected to each of the semiconductor chips by press contact. The above integrated bodies of electrodes and semiconductor chips are inserted between a first common main electrode plate (Cu) 4 and a second common main electrode plate (Cu) 5, on each surface of them an Au plated film of 2-4 μ m thick is formed. In this case, in order to absorb the variation in height, a porous copper plates 17 manufactured in a shape having a hole at the center are arranged around the pin 25 and a member 26 for insulating the pin between the intermediate electrode plate 13 and the common electrode plate 4. In accordance with this method, shifting the location of respective

porous metallic plate 17 can be prevented by the member 26 for insulating the central pin, and an assembling operation can be performed readily.

[0053] The gate circuit 27 is contained in a groove 28 provided to the first common main electrode plate (Cu) 4, taken out to the periphery of the package, and further taken out by the wire 29, 23 to outside the package. In order to decrease the contacting resistance further, a complex porous copper plate was utilized as the porous metallic plate in the present embodiment. The complex porous copper plate has a structure as shown in FIG. 17, wherein a dense copper foil was integrated onto the surface of the porous plate. Accordingly, the contacting resistance between the porous metallic plate and the intermediate electrode plate, and the common electrode plate could be decreased significantly. The above effect was remarkable in the region where the pressure was small, and the contacting resistance could be decreased from 1/5 to 1/10. Variation in thickness at each position of the chips mounted practically in the present embodiment was 200 μm at maximum. However, results of determining pressure distribution by inserting pressure sensitive paper between the intermediate electrode plate 14 and the common main electrode plate 5 revealed that the pressure difference was small, and they were pressed almost uniformly.

[0054] As explained above, in the case when various kinds of semiconductor chips are arranged in parallel and mounted in a package, and their thickness are varied significantly depending on their kind, a following method is effective; that is, the intermediate electrode plates having various average thickness depending on the kinds of the chips are prepared; large difference of the thickness of the chips are adjusted with the intermediate electrode plates; furthermore, the porous metallic plate of the present invention is used for accommodating the variation in height of the intermediate electrode plates and the semiconductor chips.

[0055] FIG. 21 indicates an embodiment, wherein a porous copper plate 30, on which surface a dense thin film layer 33 of Ag is formed as a body, is arranged between cathode electrode side of a wafer size semiconductor element 31 and an intermediate electrode plate 32. A metal foil 34 made of Mo and an intermediate electrode plate 35 plated with Ag, respectively, were arranged between anode electrode side of the semiconductor element 31 and a common electrode plate 5. The porous copper plate had an average void diameter of approximately 0.1 mm, cell number of 40 pieces/mm^2, thickness of metallic channel of 30-50 μm, plate thickness of 0.8 mm, and void fraction of approximately 75 %. In accordance with the porous copper plate 30, variation of height is absorbed, and the contacting resistance can be decreased by compensating the decrease in contacting area based on voids at the surface of the porous metal.

[0056] FIG. 22 indicates an embodiment, wherein no intermediate electrode plate is inserted between a collector side electrode of the semiconductor chip 1 and a common electrode plate. In order to prevent rupture of the semiconductor element by pressing when the intermediate electrode plate at collector side is omitted, and a porous metallic plate was arranged between the common electrode plate 5 and the semiconductor element 1, it is important that the porous metallic plate 36 is arranged in a region same or smaller than the shape of the intermediate electrode plate 2, on which surface a soft metal film 38 is formed. In accordance with the present embodiment, a soft metal foil 37 is inserted between a chip main electrode and the porous metallic plate, in order to decrease further contacting resistance and to protect the chips.

[0057] Conventionally, surface of the common electrode plate, and the intermediate electrode plate have been necessarily finished to make their maximum surface roughness (Rmax) less than 1 μm, in order to decrease their contacting resistance. However, even if surface of the common electrode plates and the intermediate electrode plates, which interposes the porous metallic plate, soft metal foil, and the like is coarse such that its maximum surface roughness (Rmax) exceeds 1 μm, the material is deformed matching with uneven shape of the surface, and contacting area is increased microscopically and contacting resistance can be decreased. Therefore, production cost can be decreased.

[0058] As the material for the porous metallic plate, metals mainly such as Cu, Al, Ag, Au, Ni, and the like, or their alloy are desirable. Based on using state of the semiconductor device, it is desirable to select optimum material and surface treatment in consideration of priority of decreasing the thermal resistance and electrical resistance, and improving deformation capability.

[0059] As the material for the intermediate electrode, a material having a thermal expansion coefficient at a middle of Si and a material of the external main electrode, and a desirable thermal conductivity and electrical conductive is used. Practically, a single metal such as tungsten (W), molybdenum (Mo), or complex material or alloys containing these element as a main composition material such as Cu-W, Ag-W, Cu-Mo, Ag-Mo, Cu-FeNi, and the like, a complex material of metal with ceramics or carbon, for instance, such as Cu/SiC, Cu/C, Al/SiC, Al/AlN, and the like are desirable. On the other hand, as the material for main electrode, a conductive material having a desirable thermal conductivity such as copper, aluminum, and their alloys, or the above complex materials are desirable.

[0060] The mounting method of the present invention can be applied naturally to the press contact type semiconductor devices composed of no diode, but only switching semiconductors such as IGBT and the like. Additionally, the mounting method of the present invention is naturally effective in mounting, for instance, a large number of diodes in a press contact type package by the above method. Furthermore, the above embodi-

ments are explained using mainly IGBT, but targets of the present invention are all the semiconductor elements comprising at least a first main electrode on a first main plane and a second main electrode on a second main plane. Therefore, the present invention can be applied to the insulated gate type transistors (MOS transistor) other than the IGBT, the insulated gate type thyristors (MOS controlled thyristor) including IGCT (Insulated Gate Controlled Thyristor) , GTO, thyristors, and diodes, and others in a similar way. Furthermore, the present invention is effective to the compound semiconductor elements such as SiC other than Si element, GaN, and the like.

[0061] In accordance with the press contact type semiconductor devices of the present invention, stable contact conditions between electrodes can be obtained even if their size is increased (increasing capacity), so semiconductor devices having low electrical resistance and low thermal resistance can be obtained. Accordingly, a large capacity converter, of which converter volume and cost are reduced remarkably, can be realized by using the press contact type semiconductor device of the present invention. A composition circuit diagram of one bridge, in a case when the press contact type semiconductor devices of IGBT relating to the present invention are applied as main converting elements to a converter for power, is indicated in FIG. 23. The IGBT elements 40 as the main converting elements and diode elements 41 are arranged in reverse parallel, and the converter is composed by connecting n pieces of these elements in series. These IGBT and diodes indicate the press contact type semiconductor device, wherein a large number of semiconductor chips are mounted in parallel, by the present invention. In cases of the reverse conductive IGBT press contact type semiconductor devices in embodiments of the present invention indicated in FIG. 7 - FIG. 9, and FIG. 18 - FIG. 20, the IGBT chips and the diode chips in the figures are assembled and contained in a package. Additionally, snubber circuits 42 and a current limiting circuit are added to the above assembly. A composition of self-commutated converter using four bridges of the three phase bridge indicated in FIG. 23 is indicated in FIG. 24. The press contact type semiconductor devices of the present invention are mounted in a shape called a stack structure, wherein a plurality of the semiconductor devices connected in series interposing water-cooled electrodes in a shape to contact with outer side plane of the main electrode plate, and the whole stack is pressed together. In accordance with the present invention, uniform contact can be obtained with lower pressure than conventional products. Therefore, an effect to simplify the above stack structure and the like can be realized.

[0062] The press contact type semiconductor device of the present invention is particularly preferable not only for the above embodiments, but also for self-commutated large capacity converters using for power systems, and for large capacity converter using for mill. Furthermore, the press contact type semiconductor device of the present invention can be used for variable speed pumped storage power plant, substation facilities in building, substation facilities for railway, sodium-sulfur (NaS) battery systems, and converter for traction and the like.

[0063] In accordance with the present invention, uniform press contact state in a large area region, which has been becoming more difficult with increasing the size of package accompanied with increasing the diameter of wafer and increasing the number of chips connected in parallel in an element corresponding to increasing the capacity, can be easily realized with a relatively low pressure. That is, the variation in height of the contacting plane can be absorbed sufficiently, and thermal resistance and electrical resistance at contacting boundary planes can be decreased.

Claims

1. A press contact type semiconductor device comprising:

   a pair of main electrode plates (4, 5),
   at least a semiconductor element (1, 11, 12, 31) assembled in an interval between said pair of main electrode plates, which comprises:
   at least a first main electrode on a first main plane, and
   a second main electrode on a second main plane; and
   a metallic body (6, 9, 10, 17, 34, 35, 42, 44) having macroscopic vacancies in its internal portion, being arranged between the main electrode of said semiconductor element and said main electrode plate.

2. A press contact type semiconductor device comprising:

   a pair of main electrode plates (4, 5),
   at least a semiconductor element (1, 11, 12, 31) assembled in an interval between said pair of main electrode plates, which comprises:
   at least a first main electrode on a first main plane, and
   a second main electrode on a second main plane;
   a conductive intermediate electrode plate (2, 3, 13, 14, 32, 33) arranged between the main electrode of said semiconductor element and the main electrode plate facing to the main electrode of said semiconductor element, and
   a metallic body (6, 9, 10, 17, 34, 35, 42, 44) having macroscopic vacancies in its internal portion, being arranged between said intermediate electrode plate and said main electrode plate.

3. A press contact type semiconductor device as claimed in any of claims 1 and 2, wherein said metallic body (6, 9, 10, 17, 34, 35, 42, 44) is any one selected from the group consisting of metallic netting, metallic plate manufactured to be uneven, and porous metallic plate.

4. A press contact type semiconductor device comprising:

a pair of main electrode plates (4, 5),
at least a semiconductor element (1, 11, 12, 31) assembled in an interval between said pair of main electrode plates (4, 5), which comprises:
at least a first main electrode on a first main plane, and
a second main electrode on a second main plane; and
any one selected from the group consisting of metallic netting, metallic plate manufactured to be uneven, and porous metallic plate, being arranged between said semiconductor element, preferably its main electrode and said main electrode plate.

5. A press contact type semiconductor device comprising:

a pair of main electrode plates (4, 5),
at least a semiconductor element (1, 11, 12, 31) assembled in an interval between said pair of main electrode plates, which comprises:
at least a first main electrode on a first main plane, and
a second main electrode on a second main plane;
a conductive intermediate electrode plate (2, 3, 13, 14, 32, 33) arranged between the main electrode of said semiconductor element and the main electrode plate facing to the main electrode of said semiconductor element, and
any one selected from the group consisting of metallic netting, metallic plate manufactured to be uneven, and porous metallic plate, being arranged between said intermediate

electrode plate and said main electrode plate.

6. A press contact type semiconductor device as claimed in any of claims 1 to 5, wherein said metallic body (6, 9, 10, 17, 34, 35, 42, 44) having macroscopic vacancies in its internal portion is made of any material selected from the group consisting of Cu, Al, Ag, Au, Ni, and alloys comprising any one of the above elements as a main component.

7. A press contact type semiconductor device as claimed in any of claims 1 to 6, wherein a dense metallic layer made of a metal which is more oxidation resistant, or softer than said material is formed on surface of at least one side of said metallic body having macroscopic vacancies in its internal portion.

8. A press contact type semiconductor device as claimed in any of claims 1 to 7, wherein a soft metallic foil (45) is arranged between at least one of contacting planes facing each other of said main electrodes of the semiconductor element (1, 11, 12, 31), said intermediate electrode plates (2, 3, 13, 14, 32, 33), and said main electrode plates (4, 5).

9. A press contact type semiconductor device as claimed in any of claims 1 to 8, wherein a soft metallic film (15, 16, 45) is formed on at least one plane of said intermediate electrode plates (2, 3, 13, 14, 32, 33), or said main electrode plates (4, 5).

10. A press contact type semiconductor device as claimed in any of claims 1 to 9, wherein at least one of planes of said main electrode plates (4, 5) and said intermediate electrode plates (2, 3, 13, 14, 32, 33), is manufactured to be rugged with a maximum surface roughness (Rmax) exceeding 1 μm.

11. A power converter using a press contact type semiconductor device in accordance with any of claims 1 to 10 as a main converting element.

FIG. 1

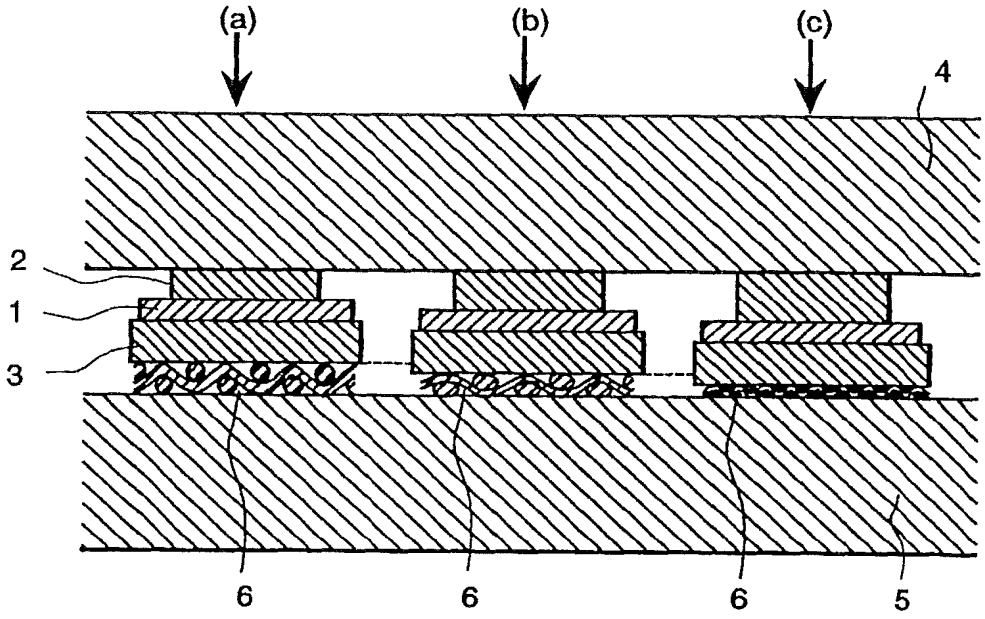
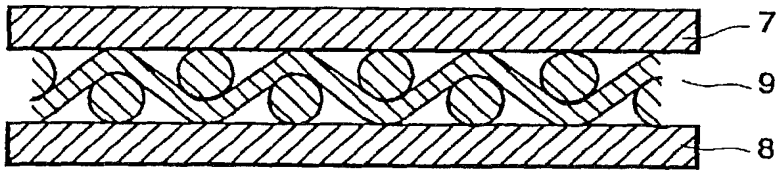
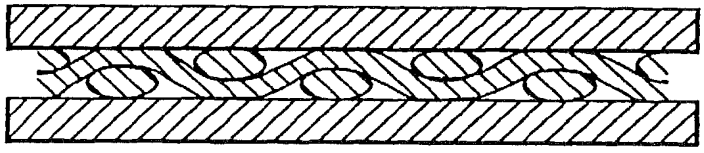


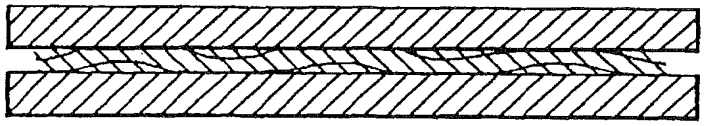
FIG. 2



(a)



(b)



(c)

FIG. 3

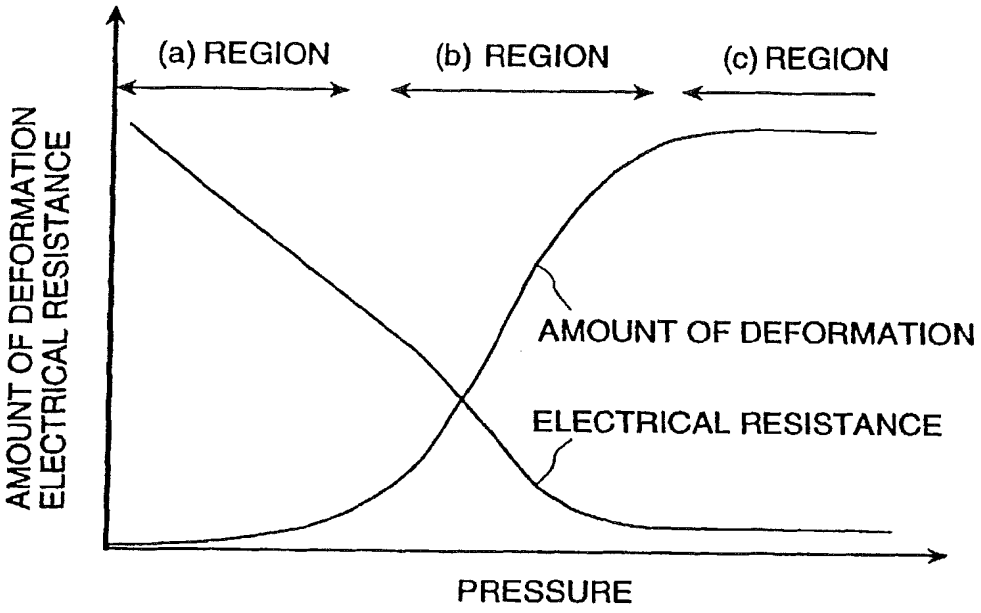


FIG. 6

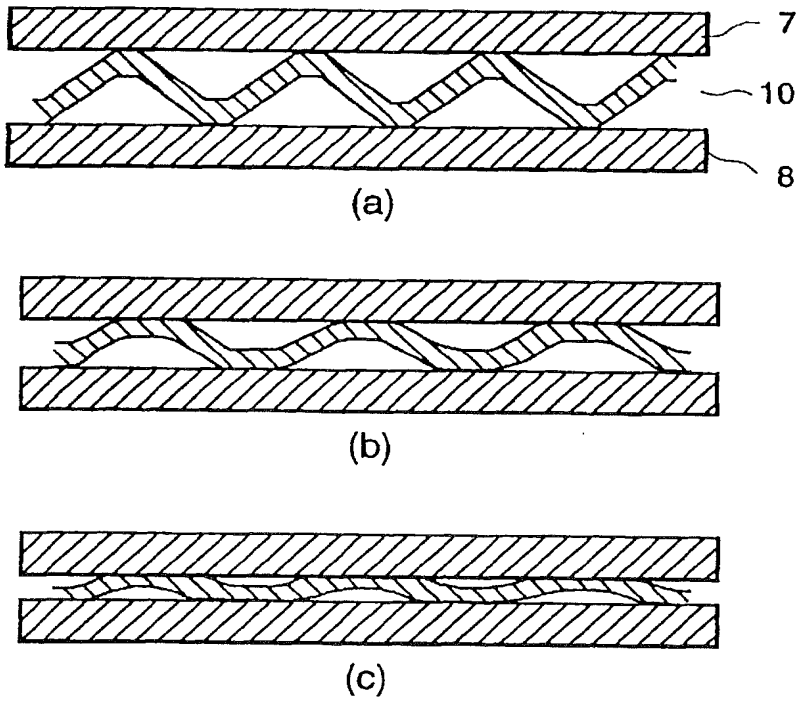
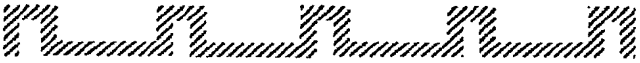


FIG. 4

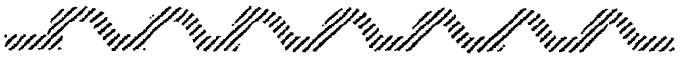
(a) 

(b) 

(c) 

(d) 

(e) 

(f) 

(g) 

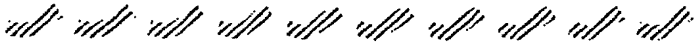
(h) 

FIG. 5

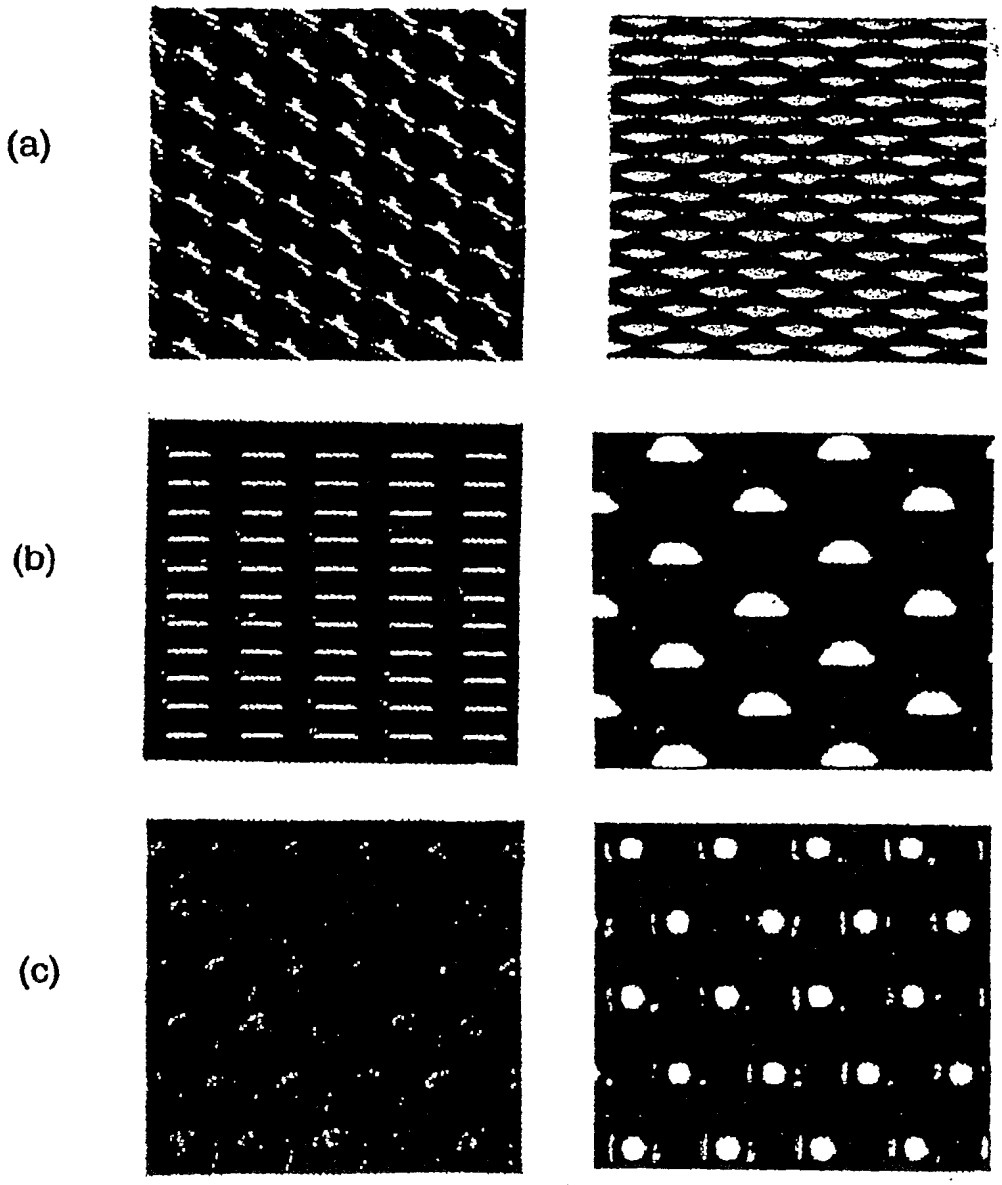


FIG. 7

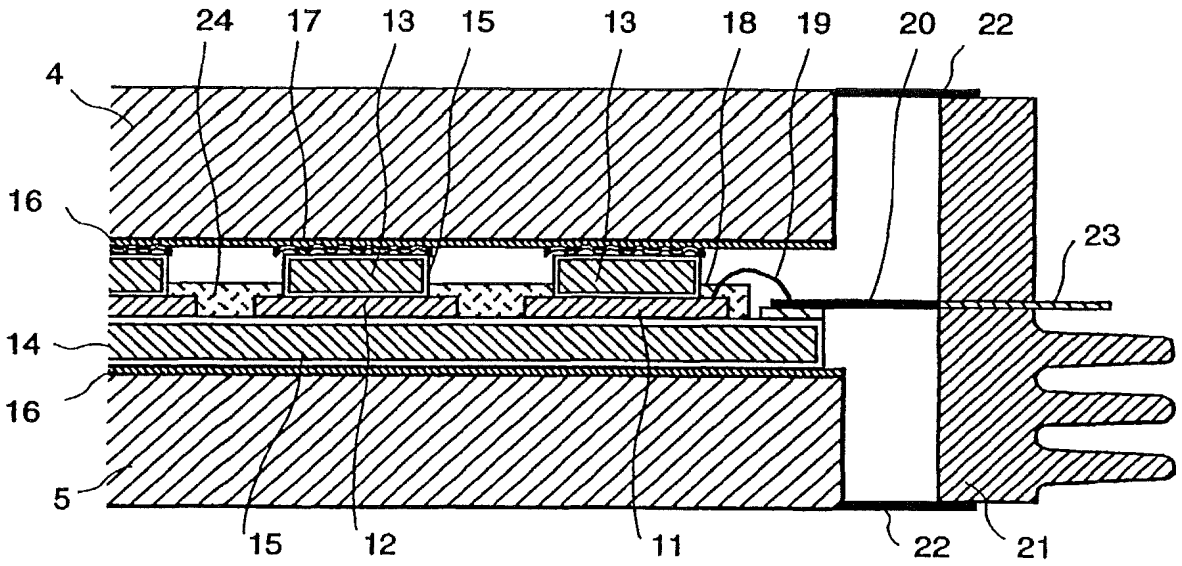


FIG. 8

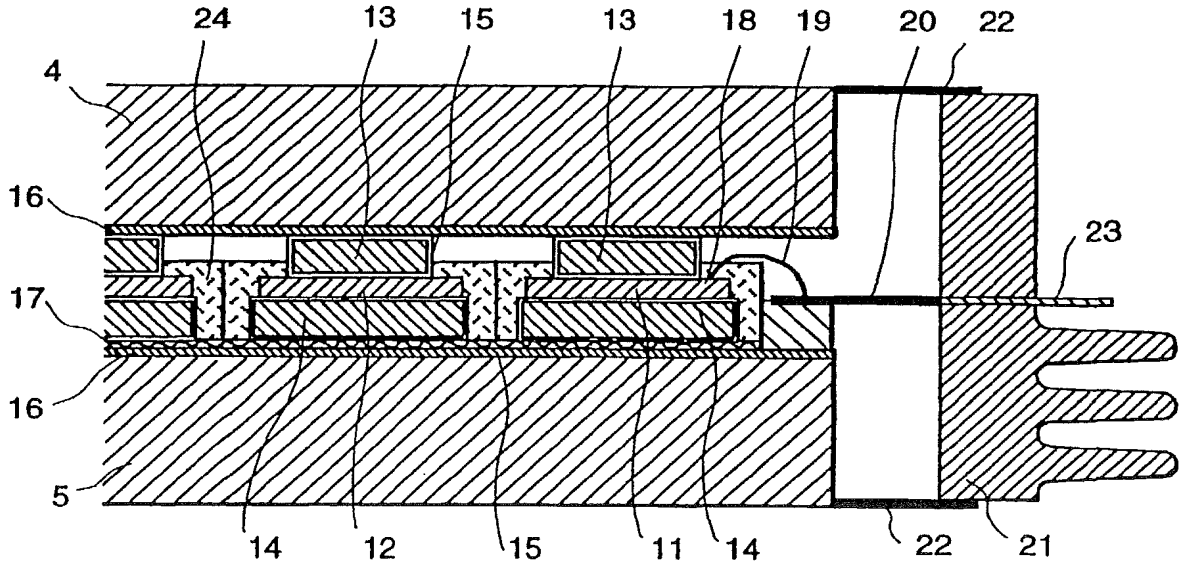


FIG. 9

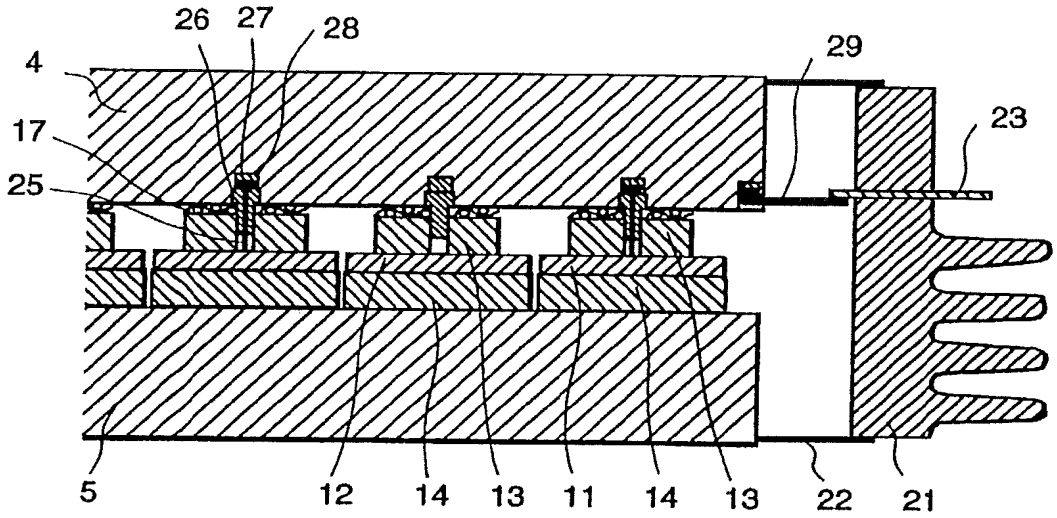


FIG. 10

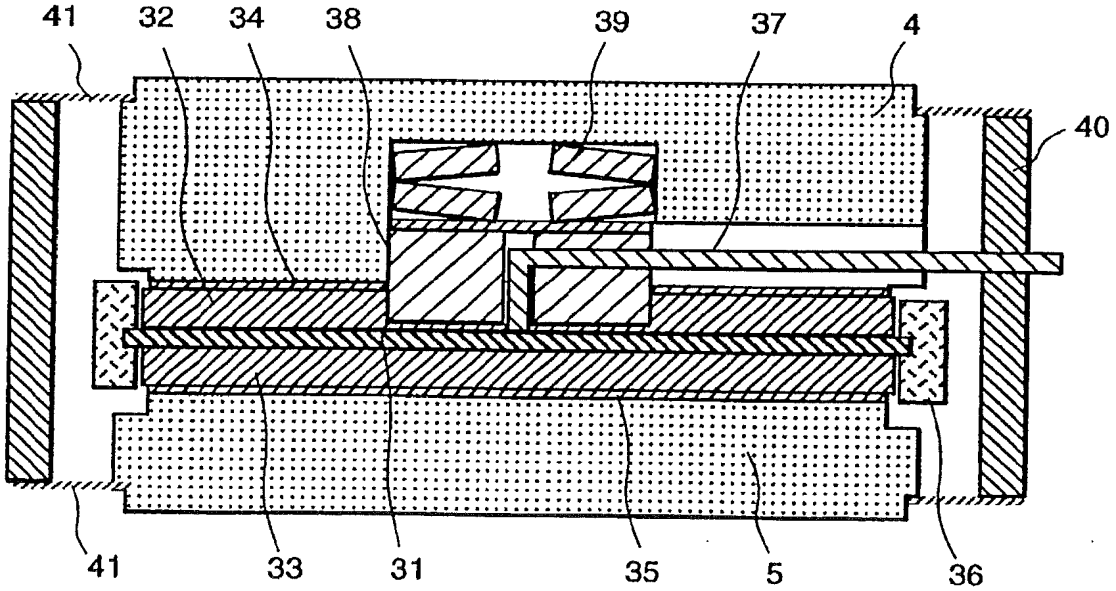


FIG. 11

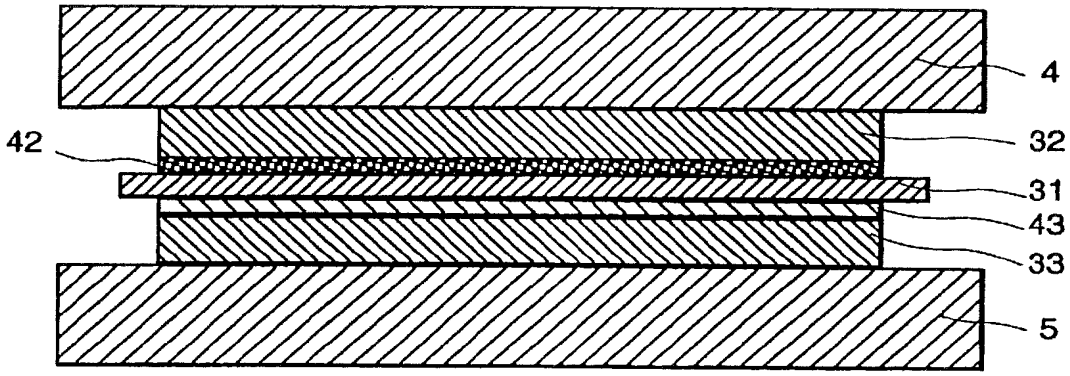


FIG. 12

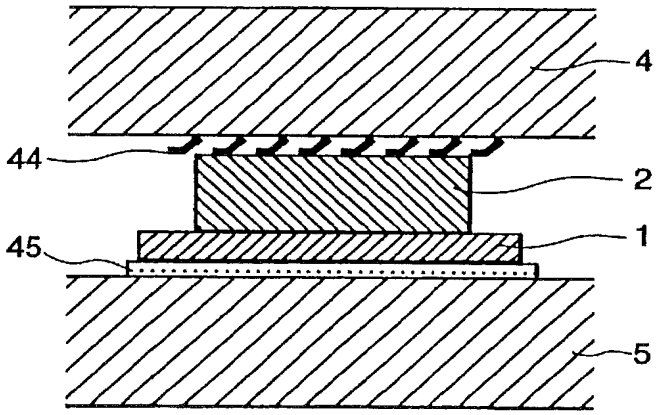


FIG. 13

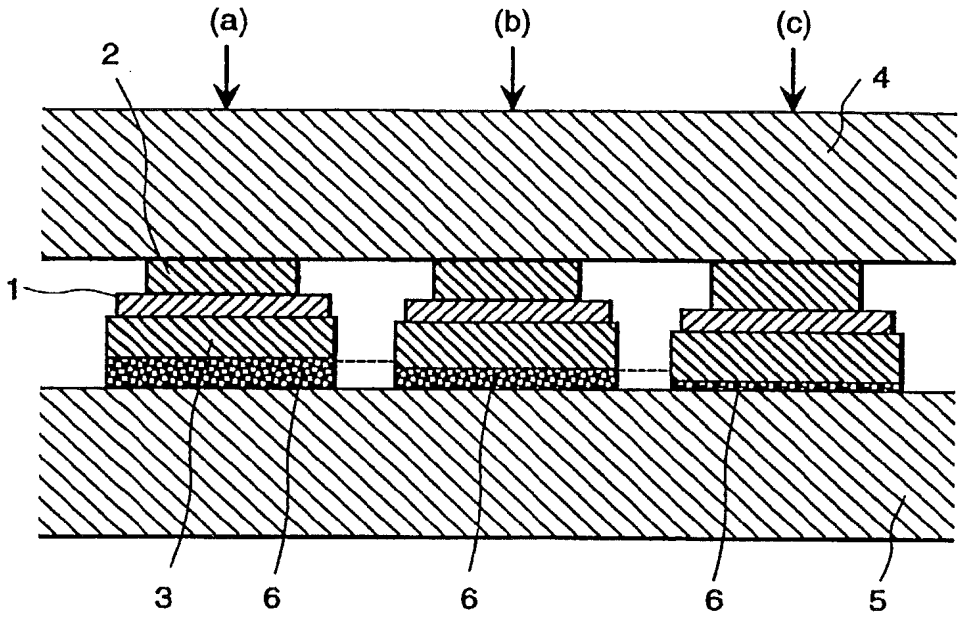


FIG. 14

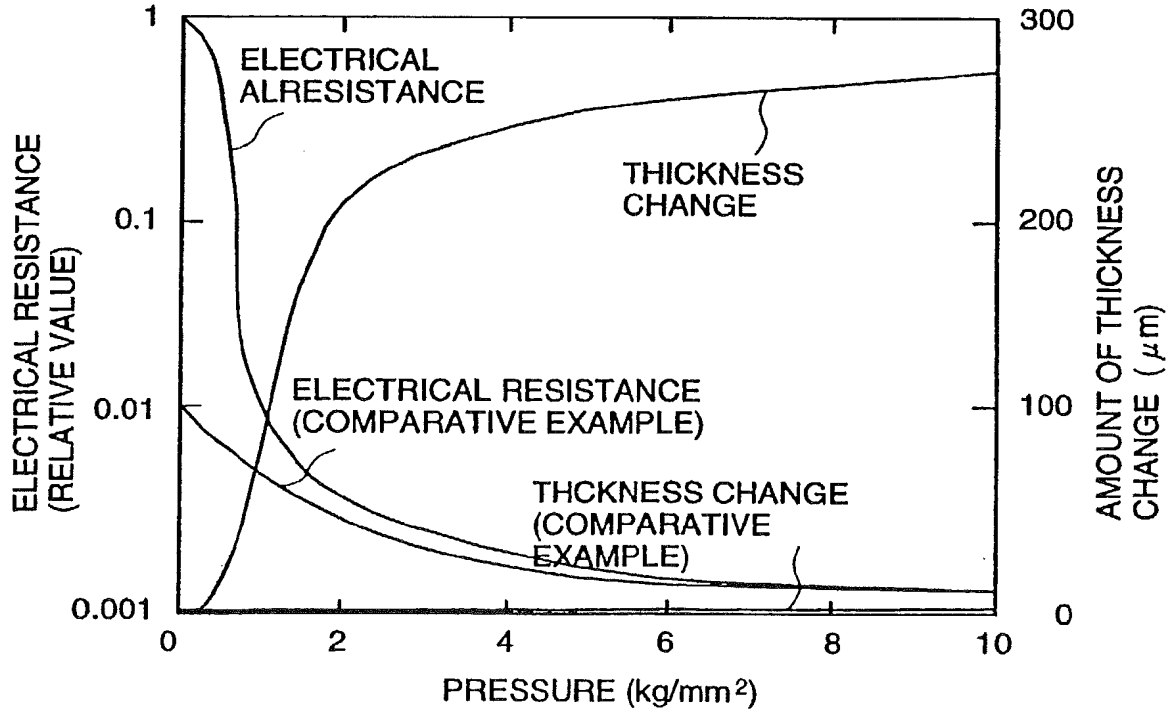
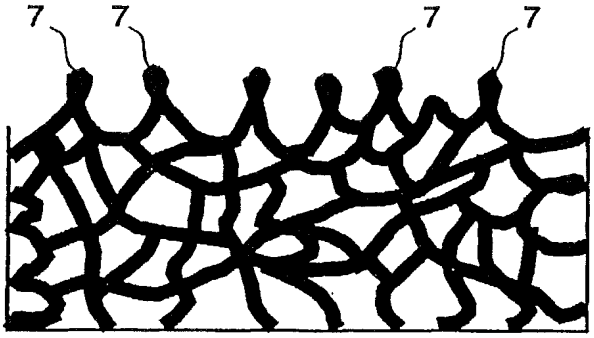


FIG. 15

(a)



(b)

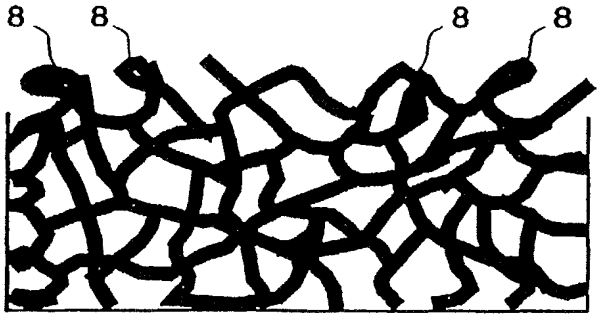


FIG. 16

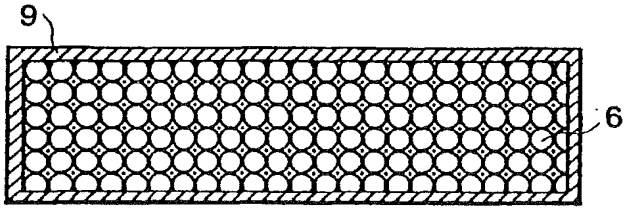


FIG. 17

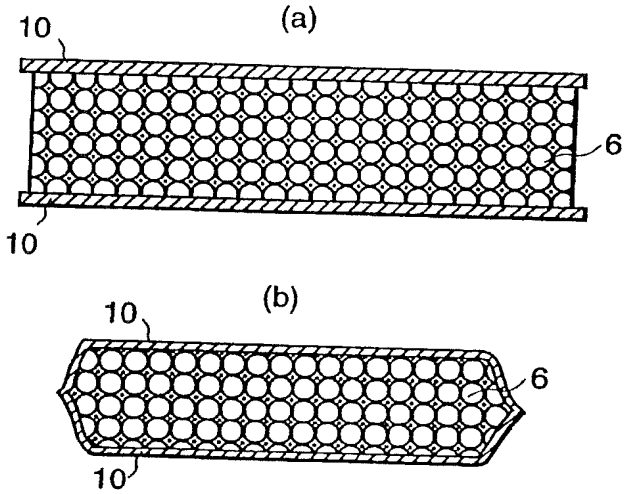


FIG. 18

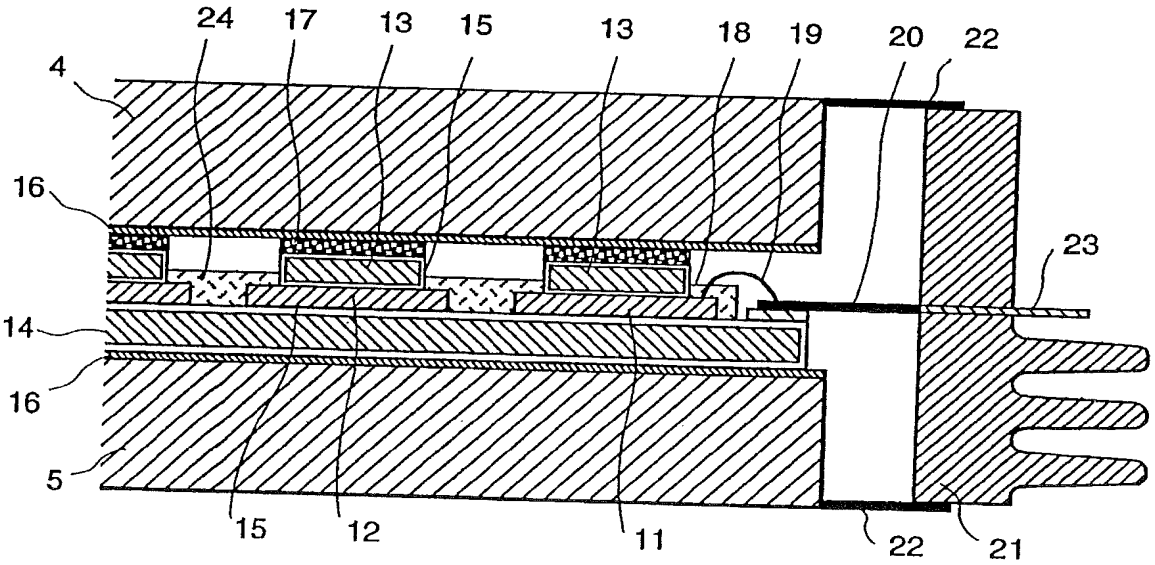


FIG. 19

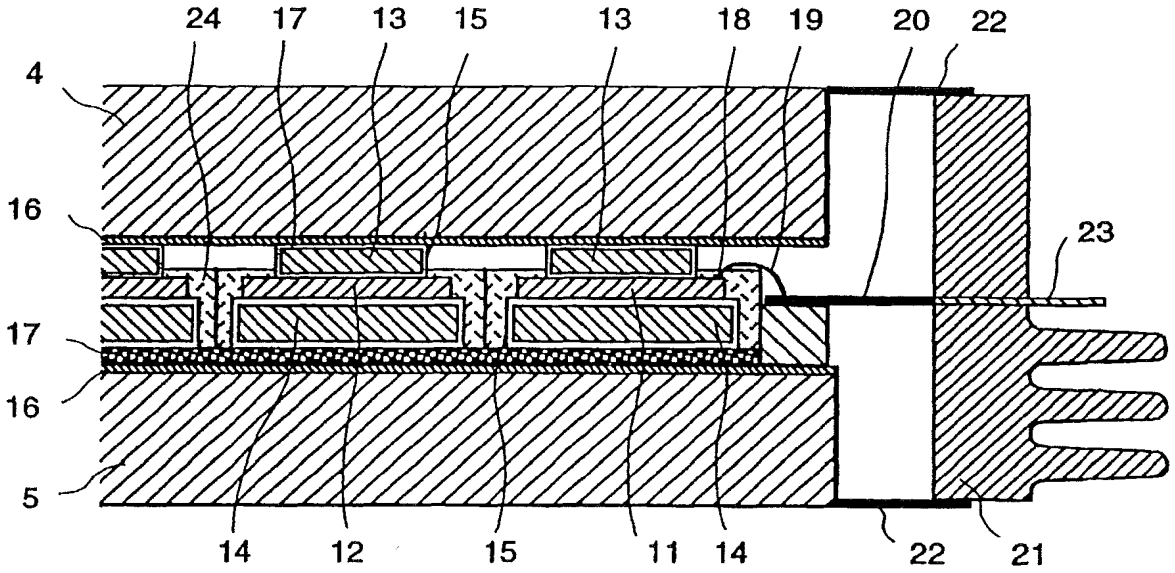


FIG. 20

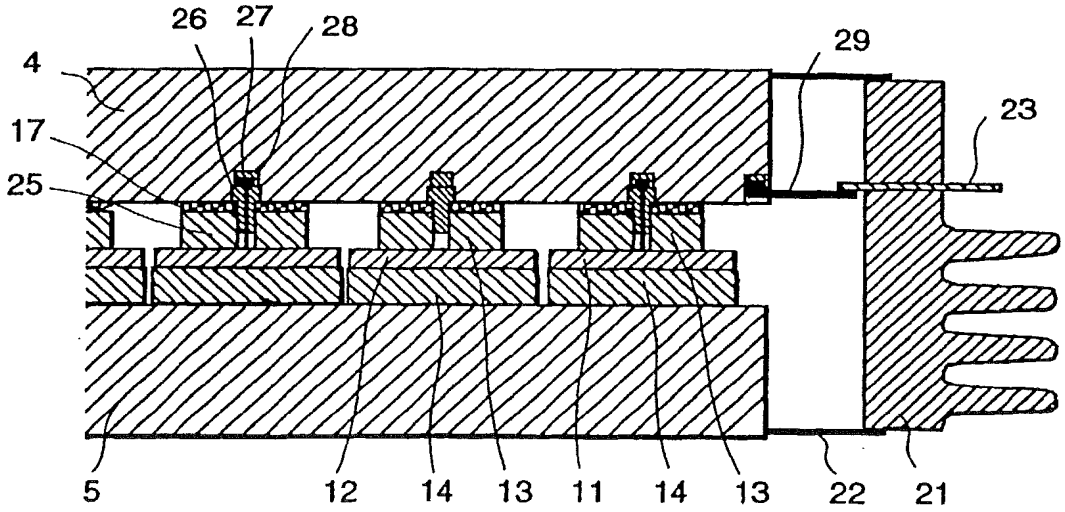


FIG. 21

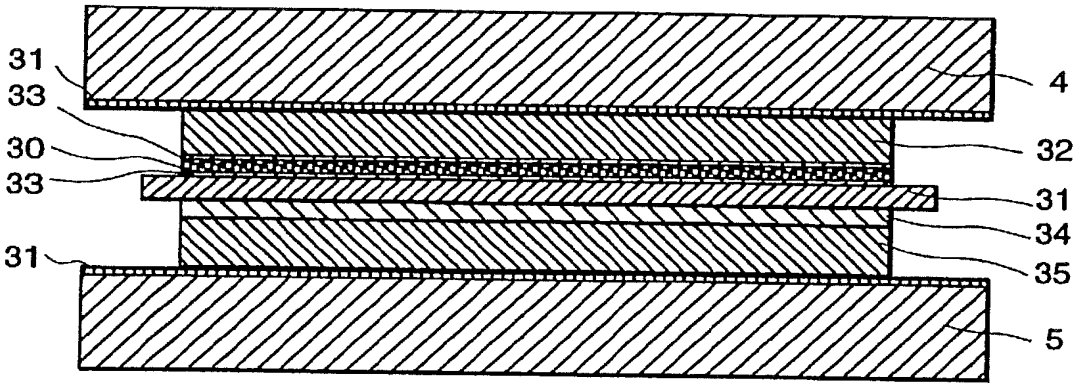


FIG. 22

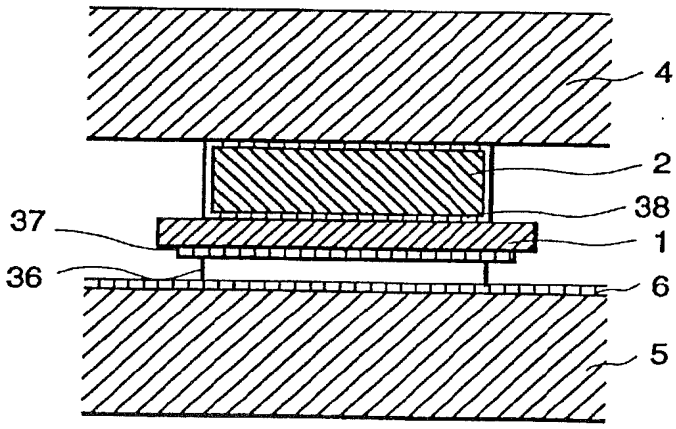


FIG. 23

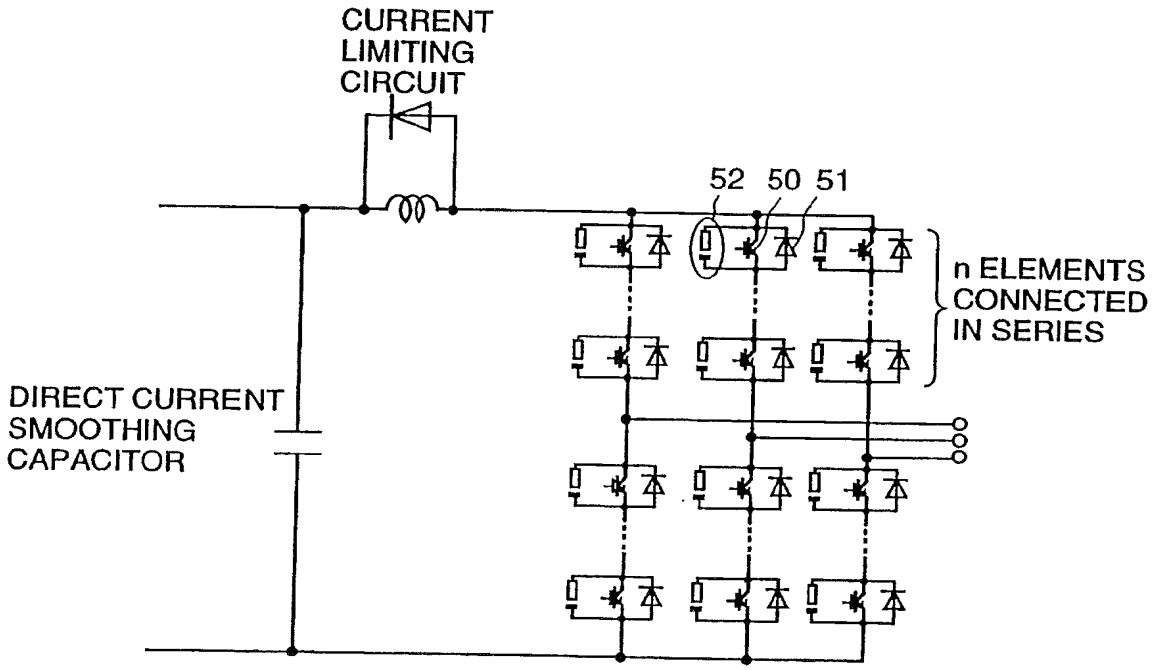


FIG. 24

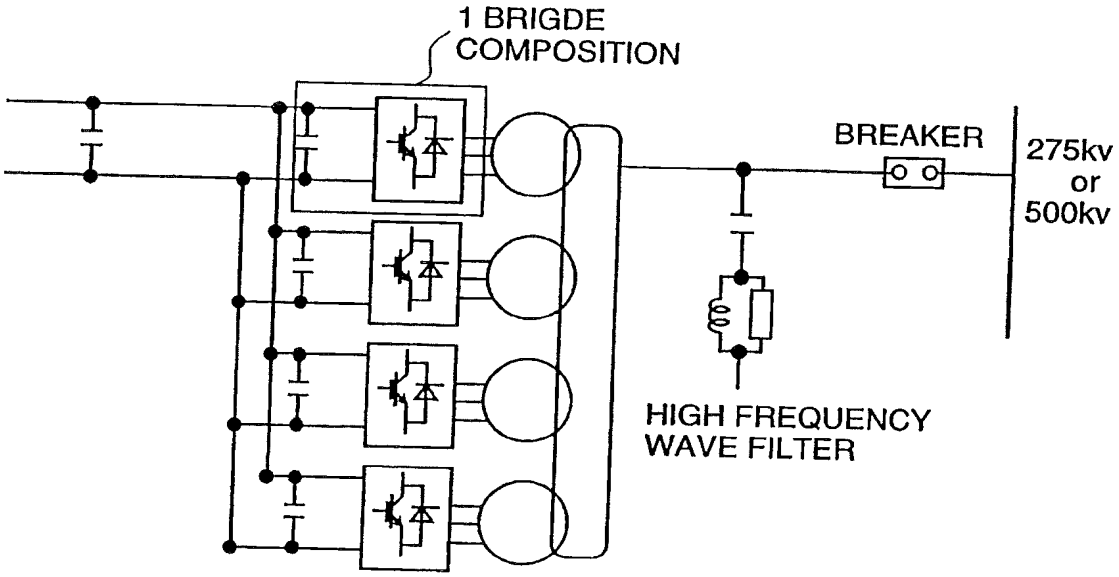
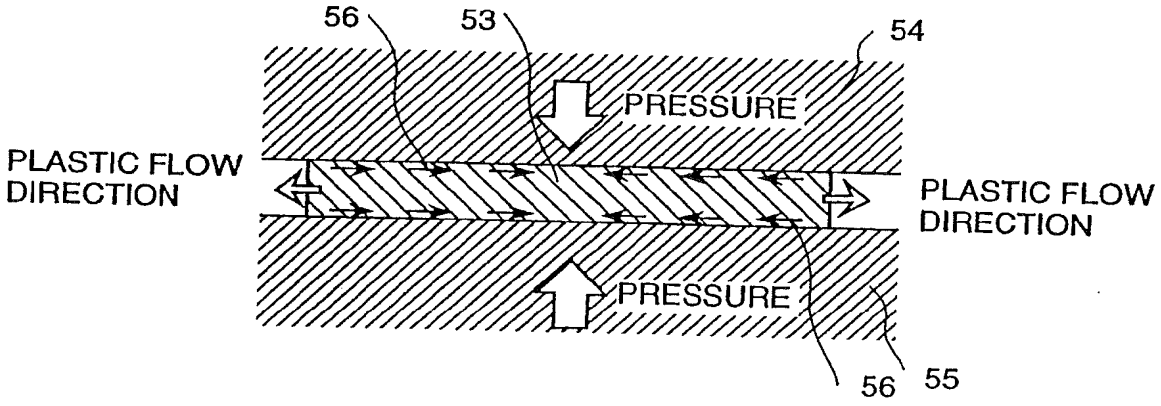


FIG. 25



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12.08.1998 JP 22784798

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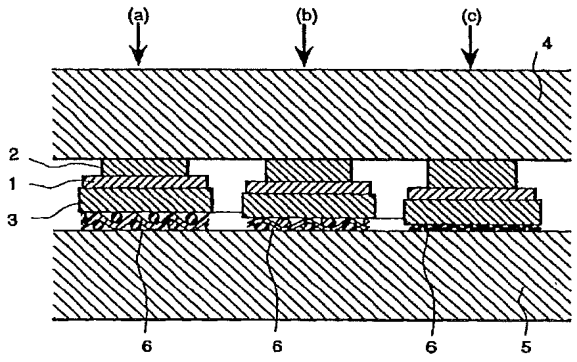
(54) Press contact type semiconductor device and converter using same

(57) In accordance with a press contact type semiconductor device, a metallic body 6 having macroscopic vacancies in its portion is arranged between a main electrode of the semiconductor device and a main electrode plate 5, or between an intermediate electrode plate 3 arranged on a main plain of the semiconductor element 1 and a main electrode plate 5, respectively.

FIG. 1



EP 0 932 201 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 99 10 0944

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	1 February 2000	De Raeve, R

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Thin Solid Films, *104* (1983) 81–87

ZrN DIFFUSION BARRIER IN ALUMINUM METALLIZATION SCHEMES*

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(Received October 7, 1982; accepted November 23, 1982)

We have studied reactively sputtered ZrN, the most thermally stable of the refractory metal nitrides, for its diffusion barrier properties in aluminum metallization schemes with Rutherford backscattering spectroscopy and transmission electron microscopy (TEM). We find this compound to be very effective against aluminum diffusion up to 500 °C, independently of substrate temperature during sputtering. The useful temperature range can be extended by 50 °C with proper preannealing prior to aluminum deposition. The TEM study of the ZrN grain size as a function of annealing temperature revealed that the grain size does not change significantly upon annealing and that the grains are relatively small even at the highest annealing temperatures (about 300 Å at 900 °C). In addition, for annealing temperatures of and below 500 °C large portions of ZrN films were found to be of either amorphous or extremely fine-grain material, thus inhibiting the diffusion along grain boundaries. The presence of $Zr_3Al_4Si_5$ ternary compound in samples annealed at 600 °C, as determined by X-ray analysis, may suggest that the ZrN barrier fails by decomposition of the film by aluminum.

1. INTRODUCTION

The problem of stable and reliable electrical contact to devices in integrated circuit technology is largely a problem of choosing a successful barrier against interdiffusion in thin film layers. Such a barrier layer in a contact structure is required to be a good thermal and electrical conductor and to be thermally stable, *i.e.* it must have large negative energy of formation and consequently a positive free energy of reaction with the films it separates.

Transition metal mononitrides offer a very attractive possibility for the above application[1]. Indeed, the previous studies of TaN and TiN [2–4] confirmed that thin films of these compounds are very effective as diffusion barriers during thermal treatments at temperatures up to 550 °C.

In this paper we report on the diffusion barrier properties of the most stable member of the refractory metal nitrides, ZrN. The heat of formation of ZrN, which

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0040-6090/83/$3.00

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is[5] $-\Delta H_f^{298} = 87.3$ kcal mol^{-1}, is even greater than that of TiN (80.4 kcal mol^{-1}). ZrN is also the best electrical conductor among transition metal mononitrides. The lowest resistivity reported in the literature[6] is $\rho_{ZrN} = 13.6$ μΩ cm as compared with 22 μΩ cm for TiN [7] and even 16.7 μΩ cm for $TiSi_2$ [8].

Hence, as silicide contacts require an additional layer for the diffusion barrier, it might be advantageous in many applications to replace silicides altogether in metallization schemes contemplated for the scaled down devices, provided that ZrN has a contact resistivity which is low enough for silicon integrated circuits.

2. SAMPLE PREPARATION

Films of ZrN of 800–1500 Å thickness were reactively sputtered in a planar diode r.f. sputtering system in a mixed N_2–Ar (or N_2–Kr) atmosphere. The sputter gases used were of research grade (99.9995% pure). Prior to the sputter deposition, the system was pumped down to a pressure of 2.7×10^{-7} Torr and presputtered for 1 h with N_2 and argon (or krypton) gases stabilized at a total pressure of 3×10^{-2} Torr. The inert-gas-to-N_2 pressure ratio used was (1.5×10^{-3} Torr):(28.5×10^{-3} Torr). The temperature of the wafers during sputtering was about 100 °C unless intentionally raised. Throughout this study 10 Ω cm ⟨100⟩-oriented n-type silicon as well as sapphire wafers were used as substrates. Rutherford backscattering spectrometry (RBS) and X-ray analysis, using a Seeman–Bohlin glancing-angle diffractometer and Cu Kα radiation, were used in identifying the composition of the sputtered films. For the initial characterization vitreous carbon substrates were used simultaneously with silicon (or sapphire) wafers. The reason for using such substrates is that the atomic mass of carbon is less than that of oxygen or nitrogen, so that any presence of these elements in the sputtered films can be detected with RBS. The result of such characterization is shown in Fig. 1. The flat plateau of the zirconium signal in Fig. 1 indicates that the deposited ZrN films are homogeneous in composition. A possible oxygen contamination of the as-deposited films was found to be below the detection limit of RBS, which is less than 0.1% for the case shown in Fig. 1. However, all films showed the presence of up to about 0.5% Hf which is a contaminant normally associated with zirconium because of the difficulty in separating it metallurgically. Other than this impurity, the target was 99.99% pure. The X-ray diffraction spectrum of ZrN film deposited on a single-crystal sapphire substrate is illustrated in Fig. 2. The diffraction peaks can all be identified as pertaining to ZrN. Compositional analysis of the as-deposited films with RBS combined with X-ray analysis shows that these films are of stoichiometric ZrN. The large width of the ZrN diffraction peaks points to a fine-grain microstructure. This is consistent with transmission electron microscopy (TEM) analysis of the grain size of as-deposited films. It was found that the majority of the films consisted of either amorphous material or of fine-grain (below 50 Å) polycrystalline material containing isolated islands of larger grain size material.

Annealing of ZrN films for electrical characterization as well as for the study of metallurgical interaction with neighboring aluminum, silicon and SiO_2 layers was performed in a furnace (Marshall type) flushed with purified helium. X-ray diffraction and TEM analysis were used to investigate the microstructure of the films before and after annealing. The results of the resistivity measurements will be

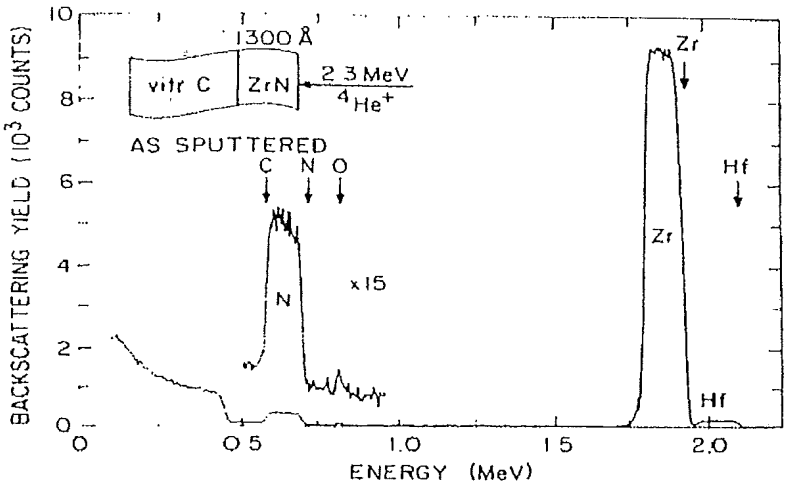

Fig. 1. 2.3 MeV $^4He^+$ spectrum of a ZrN film 1300 Å thick reactively sputtered onto a vitreous carbon substrate. The spectrum has been enlarged 15 times between 0.5 and 1 MeV. The vertical arrows indicate surface positions of the corresponding elements.

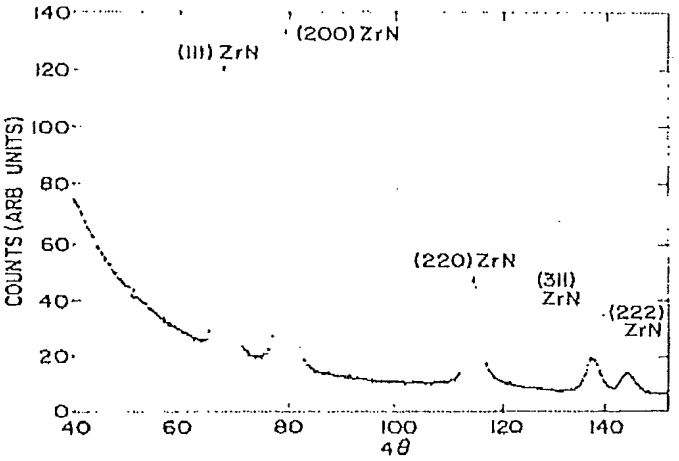

Fig. 2. Glancing-angle X-ray diffraction spectrum obtained with a Seeman–Bohlin camera and Cu Kα radiation of a ZrN layer (as sputtered) deposited on a sapphire substrate.

presented elsewhere. It is interesting to note, however, that the resistive transition of ZrN films into a superconducting state at about 7.5–8 K provided an additional check on the compositional homogeneity of the films.

3. RESULTS AND DISCUSSION

The thin film structure under study consisted of 3300 Å of aluminum evaporated on top of ZrN with a silicon wafer as a substrate. The RBS spectrum of the as-deposited structure is shown in Fig. 3(a). The origin of the signals from the different layers or their components are indicated. The vertical arrows mark the energy of α particles scattered from surface positions of the corresponding element. It is thus seen in Fig. 3(a) that both the zirconium and the silicon signals are shifted to lower energies because of the energy loss of α particles in the overlaying aluminum films. The series of isochronal anneals (t_a = 30 min) to which the samples were subjected left the RBS spectrum practically unchanged up to an annealing

temperature of 500 °C. After annealing at 550 °C for 30 min a visible change in the spectrum occurred. This is shown in Fig. 3(b). The zirconium signal has a tail extending to higher energies at 1.9 MeV and the plateau of the aluminum drops at its low energy side. These indicate that a reaction between the aluminum and ZrN films was initiated. From X-ray analysis we found that a compound, identified as Al_3Zr, was formed at the Al–ZrN interface. Further annealing at 600 °C for 30 min resulted in a spectrum as shown in Fig. 3(c). A strong interdiffusion of the individual layers has taken place as shown by the appearance of the zirconium and silicon signals at their respective surface positions. The barrier has failed completely. The diffusion barrier property of ZrN could be improved by 50 °C if the ZrN films were annealed for 30 min at 900 °C prior to the deposition of aluminum. The X-ray analysis of the failed film revealed, in addition to aluminum and ZrN, the presence of a $Zr_3Al_4Si_5$

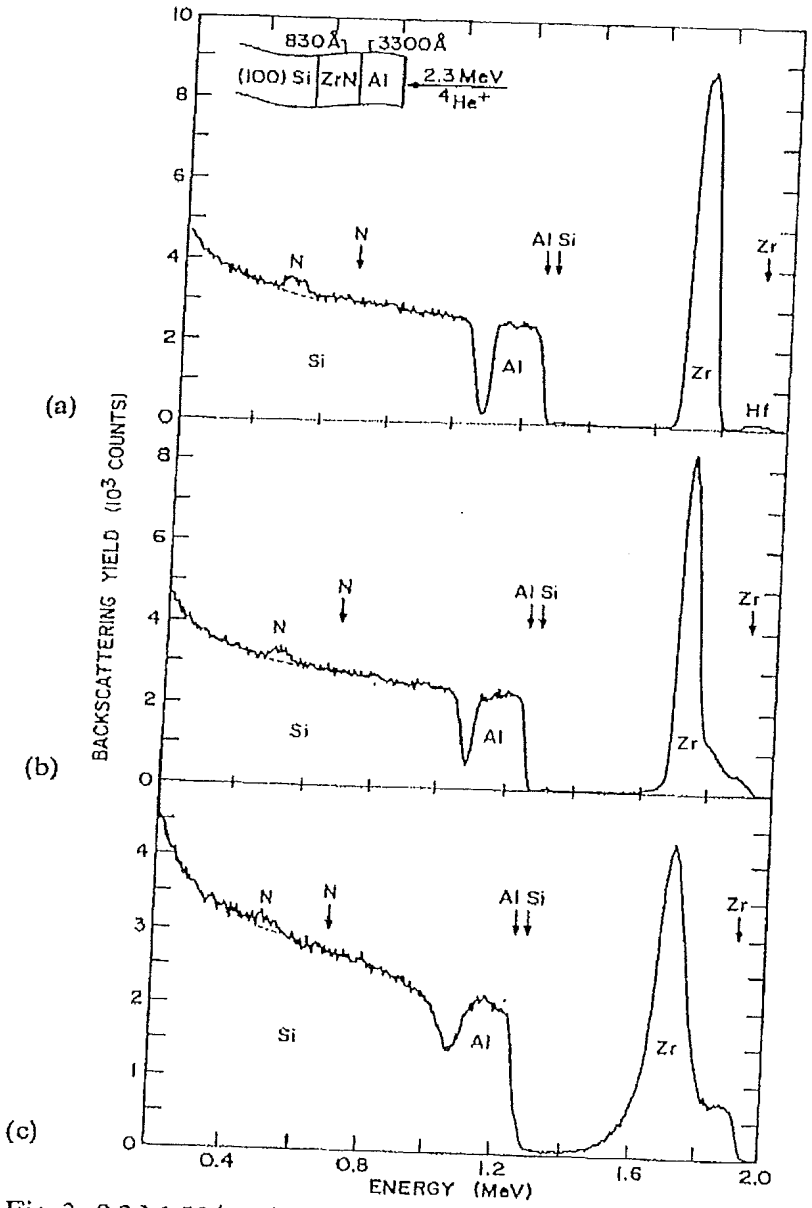

Fig. 3. 2.3 MeV $^4He^+$ RBS spectra of an Al/ZrN/Si structure: (a) after deposition; (b) following a 550 °C anneal for 30 min in helium; (c) following a 600 °C anneal for 30 min in helium. The vertical arrows indicate surface positions of the corresponding elements.

ternary compound. Furthermore, the temperature at which ZrN diffusion barrier layers failed was independent of the substrate temperature during the sputter deposition of ZrN up to at least 300 °C.

In order to have some insight into the failure mechanism of ZrN diffusion barrier layers, we first investigated whether ZrN films prevent silicon from diffusing into the surface layers. Toward this end, we evaporated 2000 Å of palladium on a ZrN film deposited on silicon. If silicon could diffuse through ZrN, we would expect to detect the presence of Pd_2Si; since the formation temperature of Pd_2Si is 250 °C [9], it would readily form at 500–600 °C. The result was negative: RBS analysis of the films shows no indication of Pd_2Si formation after annealing at 600 °C for 30 min. In addition, the ZrN interface with SiO_2 was found to be extremely stable. For films deposited on oxidized silicon substrates, the RBS spectrum remained unchanged at the highest annealing temperatures of 600 °C.

If it is not silicon that diffuses through the barrier layer to react with aluminum, thereby destroying the ZrN diffusion barrier, then it is plausible that the aluminum is responsible for the barrier failure. Wittmer[3] suggested that, in the case of titanium and tantalum nitride as well as carbide diffusion barrier films, the interaction of aluminum with the barrier layer can result in the decomposition of that layer and the formation of aluminum nitride or carbide compounds respectively. In this scenario, the high temperature failure of the barrier is due to the formation of pinholes caused by the decomposition of the nitride and subsequent compound formation.

A similar process may occur for the Al/ZrN system. Support for this hypothesis comes from a TEM study of our films as a function of annealing temperature. The measured average grain size *versus* annealing temperature is shown in Fig. 4. Results are presented for three different substrate temperatures during the sputtering of ZrN. It is not surprising that even during 900 °C anneals the grains remain relatively small (about 300 Å) and independent of the substrate temperature during sputtering if we consider the high melting temperature $T_m = 2950$ °C for ZrN. A typical TEM micrograph for the film annealed at 700 °C is shown in Fig. 5 together with the corresponding diffraction pattern. What is interesting is that for annealing temperatures below 700 °C a great part of most of the investigated films was either amorphous or of a grain size below the resolution limit of our transmission electron

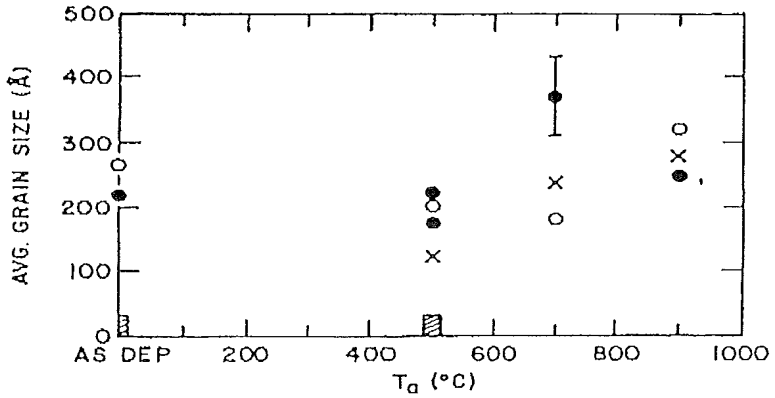

Fig. 4. Grain size of ZrN *vs.* annealing temperature for an annealing time of 30 min for three different substrate temperatures during sputtering: ●, 100–140 °C; ○, 200 °C; ×, 300 °C. The shaded areas indicate the presence of amorphous material or material with grain size below 50 Å. The vertical bar represents the width of the grain size distribution.

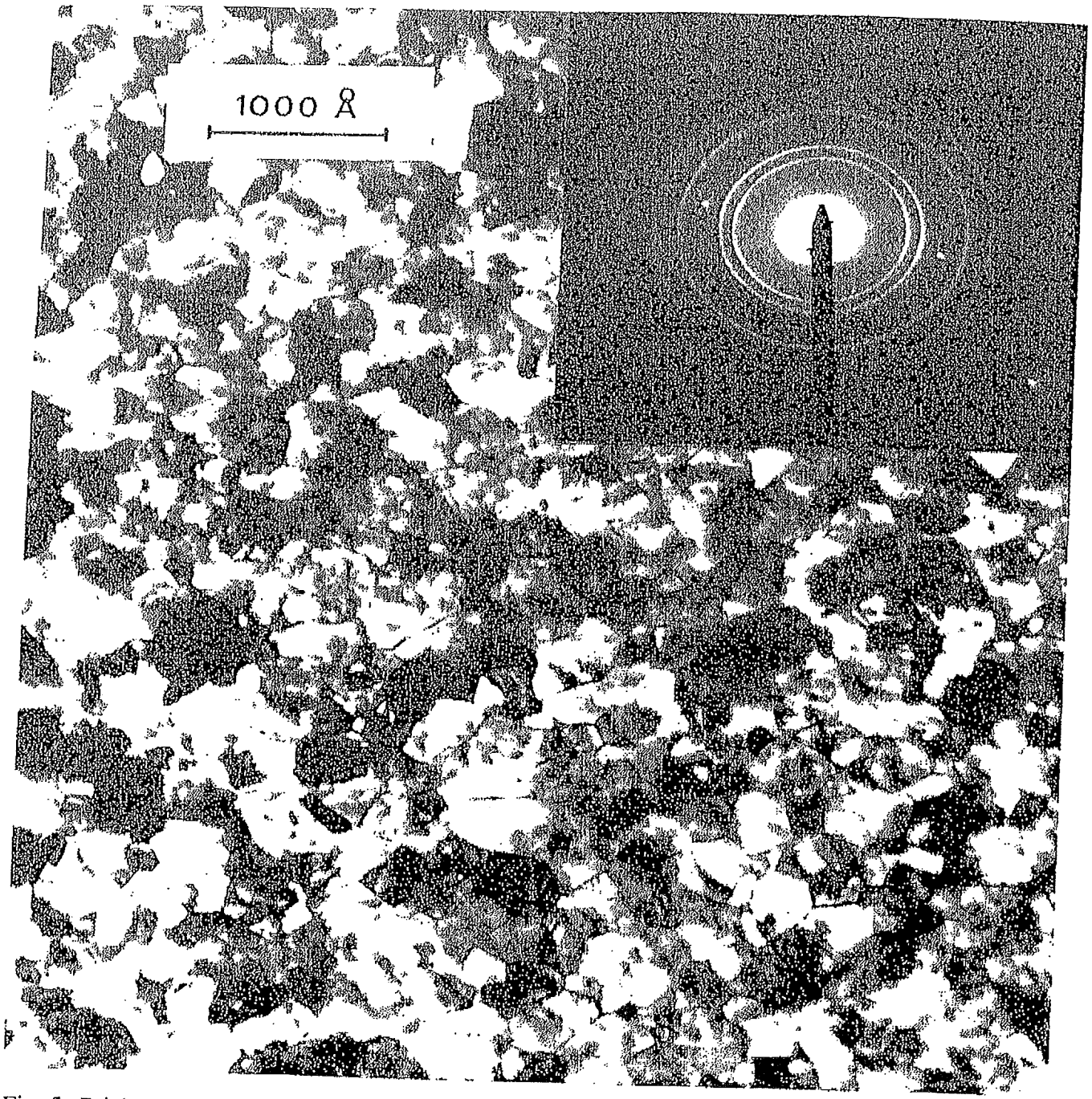

Fig. 5. Bright field micrograph and corresponding diffraction pattern of a ZrN film 1000 Å thick on silicon following annealing at 700 °C for 30 min.

microscope, although, as mentioned in the introduction, islands of larger grain material were found as well. Since diffusion in ZrN occurs mainly along grain boundaries[10] (the activation energy for bulk diffusion is greater than 4 eV [11]), aluminum (or silicon) could easily diffuse into small grain ZrN film (the average grain size of aluminum film is over 1000 Å [12]) if the boundaries are not stuffed. This would not be the case, however, if the boundaries were not continuous but were interrupted by amorphous material. The diffusion mechanism in amorphous films is different from that along grain boundaries, and the diffusion coefficient is generally

small (see for example ref. 13). Since we find that the reaction between aluminum and ZrN initiates at 500 °C, when TEM still shows the presence of amorphous material, we conclude that it is decomposition by reaction with aluminum and not interdiffusion that is responsible for the failure of ZrN as a diffusion barrier at higher temperatures.

In view of the above argument, it may seem puzzling why prebaking of the ZrN film prior to the deposition of aluminum improves its barrier property. Indeed, there is no more amorphous material present after a 900 °C anneal. The clue comes from the resistivity measurements we have performed on ZrN films. Resistivity is an extremely sensitive indicator of even the minute amounts of oxygen (not seen by RBS) present in our films, and observation of a drop of about 35% in resistivity for the films annealed at 900 °C in 6.8×10^{-7} Torr vacuum relative to the resistivity of the film annealed in a 99.999% pure helium furnace suggests that perhaps a trace amount of oxygen may stuff the grain boundaries, thus still inhibiting the diffusion. In addition, the high temperature prebaking may homogenize and improve the stoichiometry of the ZrN film. This we conclude from the decrease of the film resistivity with increasing annealing temperature in the range below 700 °C. It is conceivable that the prebaking improves the thermal stability of ZrN and thus delays the onset of the chemical reaction with the neighboring aluminum layer.

4. SUMMARIZING REMARKS

To summarize, we find that the ZrN film is an excellent barrier against aluminum and silicon diffusion through 30 min anneals at up to 550 °C. ZrN diffusion barriers fail completely at 600 °C by decomposition of the ZrN by aluminum and formation of a $Zr_3Al_4Si_5$ ternary compound.

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